High-Speed 1T 8051 Core Flash MCU, 1.25 Kbytes SRAM, 16 Kbytes Flash, 24-channel low-power high-sensitivity touch circuit, 8-level Water-Level Detection Module, LED, 12-bit ADC, 8-channel 16-bit PWM, 3 Timers, Multiplier/divider, UART, SSI, CRC

1 General description

The SC92R425B is an enhanced, industrial-grade Flash microcontroller featuring a high-speed 1T 8051 core and integrated touch keys. Its instruction set is fully compatible with traditional 8051 product families.

The SC92R425B integrates a 24-channel capacitive touch circuit with low-power operation and high sensitivity. The touch circuit can be configured to operate in STOP mode. It also integrates an 8-level Water-Level Detection Module. The SC92R425B also integrates 16 Kbytes of Flash ROM, 1.25 Kbytes of SRAM, 26 GP I/Os, 14 I/Os with external interrupt capability, three 16-bit timers, 27 channels of 12-bit high-precision ADC, eight channels of 16-bit high-performance PWM, two channels of General-Purpose PWM, internal high-frequency 10/5/1.66 MHz oscillators with ±1% accuracy and a 32K low-frequency oscillator with 4% accuracy, support for an external crystal oscillator, one UART, one three-in-one serial communication interface configurable as UART, SPI, or TWI (SSI), and a built-in LED driver supporting normal and bidirectional drive modes. To improve reliability and simplify customer circuitry, the SC92R425B also integrates highly reliable circuits, including a four-level selectable-voltage LVR and ADC reference voltage options of 1.024 V, 2.4 V, and 2.048 V. The SC92R425B offers excellent noise immunity and water-level detection performance, making it well suited for industrial control and water-level detection applications such as IoT, smart home appliances, chargers, power supplies, model aircraft, wireless communications, and game consoles.

2 Features

Operating Conditions

- Operating Voltage: 2.4 V to 5.5 V
- Operating Temperature: −40 to 105 °C

EMS

- ESD
  - HBM: JS-001-2023 Class 3A
  - MM: JEDEC EIA/JESD22-A115 Class C
  - CDM: ANSI/ESDA/JEDEC JS-002-2022 Class C3
- EFT
  - EN61000-4-4 Level 4

Package Type

- 8-pin: SOP8
- 16-pin: SOP16
- 20-pin: SOP20/TSSOP20
- 28-pin: SOP28/TSSOP28

CPU

- High-speed 1T 8051 core, fully instruction-set compatible with the 8051

Flash ROM

- 16 Kbytes Flash ROM, including a 0.5 Kbytes Fast Erase Area
- Can be written 10,000 times
- The range of the APROM Area available for IAP Operation can be set to 0K / 0.5K / 1K / all APROM through the Code Option setting

LDROM

- Stores user bootloader code
- LDROM can be set to 0K/1K/2K/4K using the Code Option setting

SRAM

- 256 bytes of on-chip directly addressable RAM
- Additional 1 Kbyte of on-chip indirectly addressable RAM
- Dedicated PWM RAM
- LED display RAM

Programming and debugging

- 2-wire JTAG Flash Programming and debugging interface: P1.2, P1.3

System Clock (f_{SYS}):

- Built-in 20 MHz high-frequency oscillator (f_{HRC})
  - When used as the System Clock Source, f_{SYS} can be programmed to 10/5/1.66 MHz using a Programmer
  - Frequency Error: ≤ ±1% across operating conditions of 2.4 V to 5.5 V and -40 to 105 ℃
- Built-in high-frequency Crystal Oscillator circuit
  - External oscillator from 2 to 16 MHz
  - When used as the system clock source, if the external high-frequency crystal frequency is less than or equal to 10 MHz, f_{SYS} can be set by the programmer to use one of the following four frequency divisions: external crystal /1, /2, /4, or /12
  - When used as the system clock source, if the external high-frequency crystal frequency is greater than 10 MHz, f_{SYS} can be set by the programmer to use one of the following three frequency divisions: external crystal /2, /4, or /12
  - An internal system clock monitoring circuit automatically switches the system clock

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source to the internal HRC if the user selects crystal oscillation as the system clock source and the crystal oscillator stops oscillating. This state is maintained until it is reset at the next reset

Internal low-frequency 32 kHz oscillator (LRC):

- Serves as the Base Timer clock source, can wake up the device from STOP mode
- Serves as the WDT clock source
- Frequency Error: Across the application conditions of 4.0 V to 5.5 V and an ambient temperature of 25 °C, the frequency error does not exceed ±4%

Low-voltage reset (LVR):

- There are 4 reset voltage options: 4.3 V, 3.7 V, 2.9 V, and 2.3 V
- Default value set by user-selected Code Option during programming

Interrupt (INT):

- Timer0 to 2, INT0, INT1, ADC, PWM, UART, SSI, Base Timer, and TK; 11 Interrupt Sources in total
- There are 2 external interrupt vectors and 14 interrupt pins; all can be configured for rising-edge, falling-edge, or dual-edge interrupts
- two interrupt priority levels

Digital Peripherals:

- 26 bidirectional, independently controllable I/O ports
  - Independently configurable pull-up resistors
  - All I/O ports have high Sink-Current Drive Capability (70 mA)
- The 16 ports LED0 to LED15 share a 16-level constant-current source
- The 16 ports LED0 to LED15 have high Sink-Current Drive Capability (150 mA)
- 11-bit watchdog timer with selectable clock prescaler
- 3 Timers: Timer0-Timer2
  - Timer2 supports the Capture function
  - Timer2 provides two Standard PWM outputs, PWM20 and PWM21
  - PWM21 can be mapped to any I/O Port
- PWM0: 8-channel 16-bit PWM
  - Can be set to independent mode or complementary mode:
    - In independent mode, all 8 PWM channels share a period, and the duty cycle can be set individually
    - In complementary mode, four pairs of complementary PWM waveforms with dead time can be output simultaneously
  - Output waveforms can be inverted and set as center-aligned or edge-aligned
- 1 independent UART communication port
  - RXD0 and TXD0 can be independently mapped to any I/O Port
- 1 SSI communication port, configurable as UART, SPI, or TWI
  - The three SSI signal lines can be independently mapped to any I/O Port
- Built-in CRC check module
- Integrated 16 × 16-bit hardware multiplier/divider

LED Drive:

- 16 LED drive pins in total: LED0-LED15
- The source drive capability of all LED pins is controlled in 16 levels
- LED0 to LED15, 16 channels in total, each providing 150 mA@0.8 V High Sink Current
- The IC System Clock (f_{SYS}) is used as the LED clock source
- After one LED scan frame is completed, the corresponding LED driver flag bit AUIF is set to 1
- The SEG output period width matches the COM width during auto-scanning
- LED dead time design requirement: between 10 µs and 3 µs
- LED supports two modes
- Bidirectional drive mode:
  - LED0 to LED11 support bidirectional drive mode, and can jointly drive up to 11 × 12 pixels
  - 12 scan modes available, from "11 X 12" to "1 X 1"
  - Common Port LED0, with 4 selectable Scan Times: 0.5T, 1T, 1.5T, and 2T
- Normal mode:
  - 8 COM and 12 SEG pins, with four COM pins multiplexed with SEG
  - Can be configured for 8 × 8, 6 × 10, 5 × 11, or 4 × 12 segment LED drive
  - Scan cycle is fixed at 1T

Analog Peripherals:

- Water-Level Detection Module
  - Software library support for highly flexible development with low development complexity
  - CMOD can only be connected externally. When connecting CMOD externally, connect a 103 Capacitor between the CMOD pin and ground
  - Supports up to 8-level Water-Level Detection
- 24-channel high-sensitivity touch circuits
  - Channels can be scanned in parallel
  - CMOD can be configured for internal or external operation. When external CMOD

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is selected, connect a 103 Capacitor between the CMOD pin and ground
  - The TK internal reference voltage can be set to a maximum level of 4 V
  - Supports Low power mode
  - Fast wake-up from STOP mode
  - Suitable for high-sensitivity touch applications, such as touchless key operation and proximity sensing
  - Complete development support: highly flexible touch software library and intelligent debugging software
- 27-channel, 12-bit ADC
  - Built-in reference voltages: 1.024 V, 2.4 V, and 2.048 V
  - ADC reference voltage options include VDD and internal 1.024 V, 2.4 V, 2.048 V
  - One internal ADC channel can directly measure the VDD voltage
  - ADC conversion complete interrupt configurable

Power-saving mode:

- Idle mode, woken up by any interrupt
- STOP mode, wake-up by INT0 to 1, BaseTimer, and TK/WL

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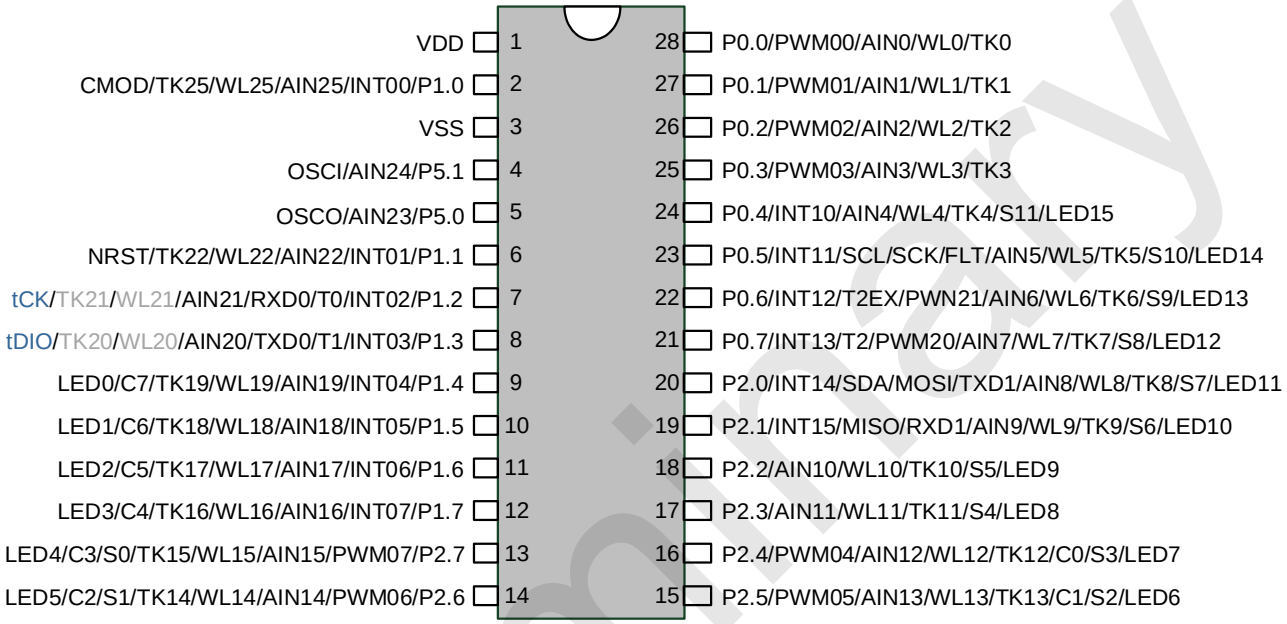
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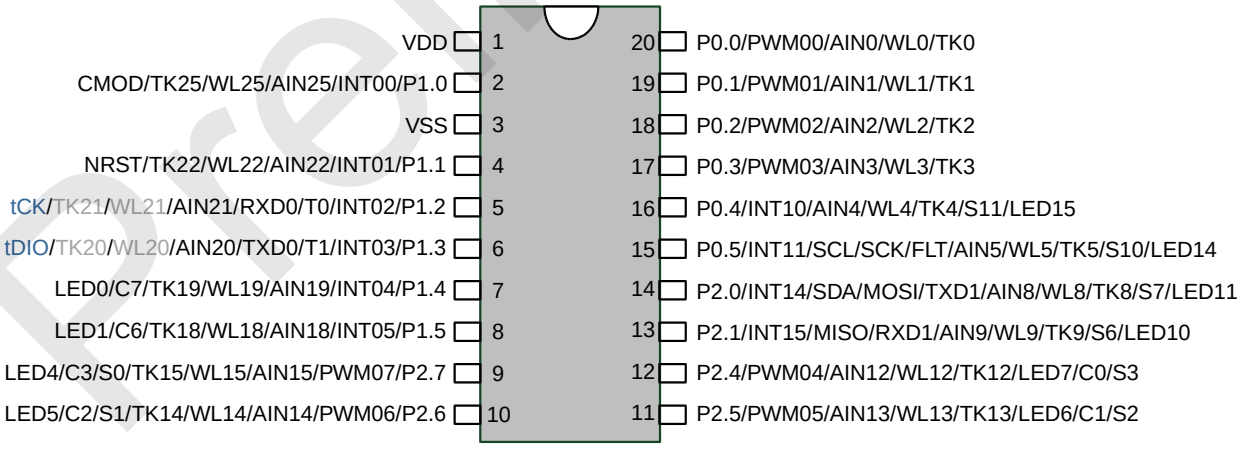
3 Pin Definition

3.1 Pin configuration

Special note: Some TK/WL Channels on the SC92R425B are multiplexed with the TK/WL debugging communication port. If the WL debugging function is required, avoid using TK20/TK21 and WL20/WL21 as much as possible!

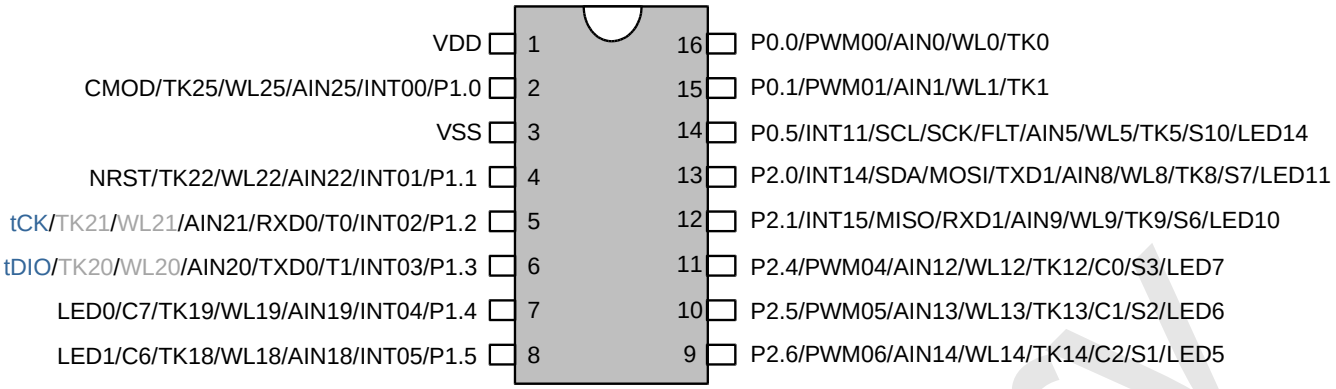


SC92R425B pin configuration diagram
For SOP28/TSSOP28 packages

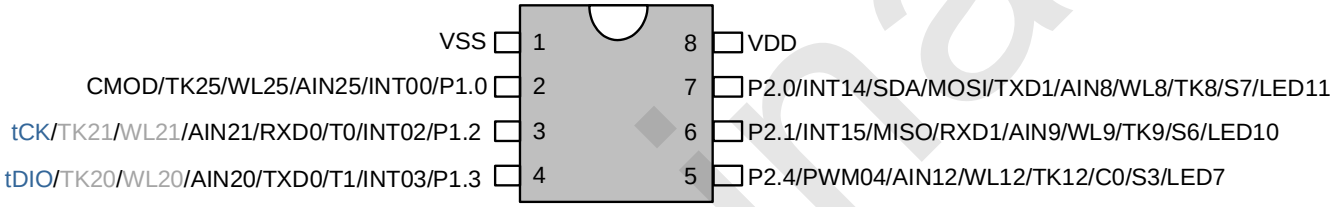


SC92R425B pin configuration diagram
For SOP20/TSSOP20 packages

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SC92R425B pin configuration diagram
For SOP16 packages



SC92R425B pin configuration diagram
For SOP8 packages

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3.2 Pin definition

Pin number				Pin name	Pin type	Function description
SOP28/ TSSOP28	SOP20/ TSSOP20	SOP16	SOP8			
1	1	1	8	V_{DD}	Power	Power Supply
2	2	2	2	**P1.0/INT00/AIN25/TK25/WL25/CMOD**	I/O	P1.0: GPIO P1.0 INT00: External interrupt 0 input 0 AIN25: ADC Input Channel 25 TK25: TK channel 25 WL25: WL channel 25 CMOD: Touch Key external capacitor (103 capacitor recommended)
3	3	3	1	V_{SS}	Power	Ground
4	-	-	-	**P5.1/AIN24/ OSCI**	I/O	P5.1: GPIO P5.1 AIN24: ADC Input Channel 24 OSCI: External Crystal Oscillator input pin
5	-	-	-	**P5.0/AIN23/ OSCO**	I/O	P5.0: GPIO P5.0 AIN23: ADC Input Channel 23 OSCO: External Crystal Oscillator output pin
6	4	4	-	**P1.1/INT01/AIN22/TK22/WL22/NRST**	I/O	P1.1: GPIO P1.1 INT01: External interrupt 0 input 1 AIN22: ADC input channel 22 TK22: TK Channel 22 WL22: WL Channel 22 NRST: External reset pin
7	5	5	3	**P1.2/INT02/T0/RXD0/AIN21/TK21/ WL21/tCK**	I/O	P1.2: GPIO P1.2 INT02: External interrupt 0 input 2 T0: Counter 0 External Input RXD0: UART0 Receive AIN21: ADC input channel 21 TK21: TK Channel 21 WL21: WL Channel 21 **If the TK/WL debugging function is required, avoid using this TK/WL channel as much as possible!** tCK: Programming and debugging port Clock line
8	6	6	4	**P1.3/INT03/T1/TXD0/AIN20/TK20/ WL20/tDIO**	I/O	P1.3: GPIO P1.3 INT03: External interrupt 0 input 3 T1: Counter 1 external input TXD0: UART0 Transmit AIN20: ADC Input Channel 20 TK20: TK channel 20 WL20: WL channel 20 **If the TK/WL debugging function is required, avoid using this TK/WL channel as much as possible!** tDIO: Programming and debugging port Data Line
9	7	7	-	**P1.4/INT04/AIN19/TK19/WL19/C7/LED0**	I/O	P1.4: GPIO P1.4 INT04: External interrupt 0 input 4 AIN19: ADC Input Channel 19 TK19: TK channel 19

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Pin number				Pin name	Pin type	Function description
SOP28/ TSSOP28	SOP20/ TSSOP20	SOP16	SOP8			
						WL19: WL channel 19 C7: LED normal mode COM output port 7 LED0: LED drive output port 0
10	8	8	-	P1.5/INT05/AIN18/TK18/WL18/C6/LED1	I/O	P1.5: GPIO P1.5 INT05: External interrupt 0 input 5 AIN18: ADC Input Channel 18 TK18: TK channel 18 WL18: WL channel 18 C6: LED normal mode COM output port 6 LED1: LED drive output port 1
11	-	-	-	P1.6/INT06/AIN17/TK17/WL17/C5/LED2	I/O	P1.6: GPIO P1.6 INT06: External interrupt 0 input 6 AIN17: ADC Input Channel 17 TK17: TK channel 17 WL17: WL channel 17 C5: LED normal mode COM output port 5 LED2: LED drive output port 2
12	-	-	-	P1.7/INT07/AIN16/TK16/WL16/C4/LED3	I/O	P1.7: GPIO P1.7 INT07: External interrupt 0 input 7 AIN16: ADC Input Channel 16 TK16: TK channel 16 WL16: WL channel 16 C4: LED normal mode COM output port 4 LED3: LED drive output port 3
13	9	-	-	P2.7/PWM07/AIN15/TK15/WL15/C3/S0/LED4	I/O	P2.7: GPIO P2.7 PWM07: PWM07 output port AIN15: ADC Input Channel 15 TK15: TK channel 15 WL15: WL channel 15 C3: LED normal mode COM output port 3 S0: LED normal mode SEG0 LED4: LED drive output port 4
14	10	9	-	P2.6/PWM06/AIN14/TK14/WL14/C2/S1/LED5	I/O	P2.6: GPIO P2.6 PWM06: PWM06 output port AIN14: ADC Input Channel 14 TK14: TK channel 14 WL14: WL channel 14 C2: LED normal mode COM output port 2 S1: LED normal mode SEG1 LED5: LED drive output port 5
15	11	10	-	P2.5/PWM05/AIN13/TK13/WL13/C1/S2/LED6	I/O	P2.5: GPIO P2.5 PWM05: PWM05 output port AIN13: ADC Input Channel 13 TK13: TK channel 13 WL13: WL channel 13 C1: LED normal mode COM output port 1

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Pin number				Pin name	Pin type	Function description
SOP28/ TSSOP28	SOP20/ TSSOP20	SOP16	SOP8			
						S2: LED normal mode SEG2 LED6: LED drive output port 6
16	12	11	5	P2.4/PWM04/AIN12/TK12/ WL12/C0/S3/LED7	I/O	P2.4: GPIO P2.4 PWM04: PWM04 output port AIN12: ADC Input Channel 12 TK12: TK channel 12 WL12: WL channel 12 C0: LED normal mode COM output port 0 S3: LED normal mode SEG3 LED7: LED drive output port 7
17	-	-	-	P2.3/AIN11/TK11/WL11/S4 /LED8	I/O	P2.3: GPIO P2.3 AIN11: ADC Input Channel 11 TK11: TK channel 11 WL11: WL channel 11 S4: LED normal mode SEG4 LED8: LED drive output port 8
18	-	-	-	P2.2/AIN10/TK10/WL10/S5 /LED9	I/O	P2.2: GPIO P2.2 AIN10: ADC Input Channel 10 TK10: TK channel 10 WL10: WL channel 10 S5: LED normal mode SEG5 LED9: LED drive output port 9
19	13	12	6	P2.1/INT15/MISO/RXD1/AI N9/TK9/WL9/S6/LED10	I/O	P2.1: GPIO P2.1 INT15: External interrupt 1 input 5 MISO: SPI Master In Slave Out RXD1: UART1 Receive AIN9: ADC Input Channel 9 TK9: TK Channel 9 WL9: WL Channel 9 S6: LED normal mode SEG6 LED10: LED drive output port 10
20	14	13	7	P2.0/INT14/SDA/MOSI/TX D1/AIN8/TK8/WL8/S7/LED 11	I/O	P2.0: GPIO P2.0 INT14: External interrupt 1 input 4 SDA: TWI SDA MOSI: SPI Master Out Slave In TXD1: UART1 Transmit AIN8: ADC Input Channel 8 TK8: TK Channel 8 WL8: WL Channel 8 S7: LED normal mode SEG7 LED11: LED drive output port 11
21	-	-	-	P0.7/INT13/T2/PWM20/AIN 7/TK7/WL7/S8/LED12	I/O	P0.7: GPIO P0.7 INT13: External interrupt 1 input 3 T2: Counter 2 External Input PWM20: PWM20 output port AIN7: ADC Input Channel 7 TK7: TK channel 7 WL7: WL channel 7 S8: LED normal mode SEG8 LED12: LED drive output port 12
22	-	-	-	P0.6/INT12/T2EX/PWM21/	I/O	P0.6: GPIO P0.6 INT12: External interrupt 1 input 2

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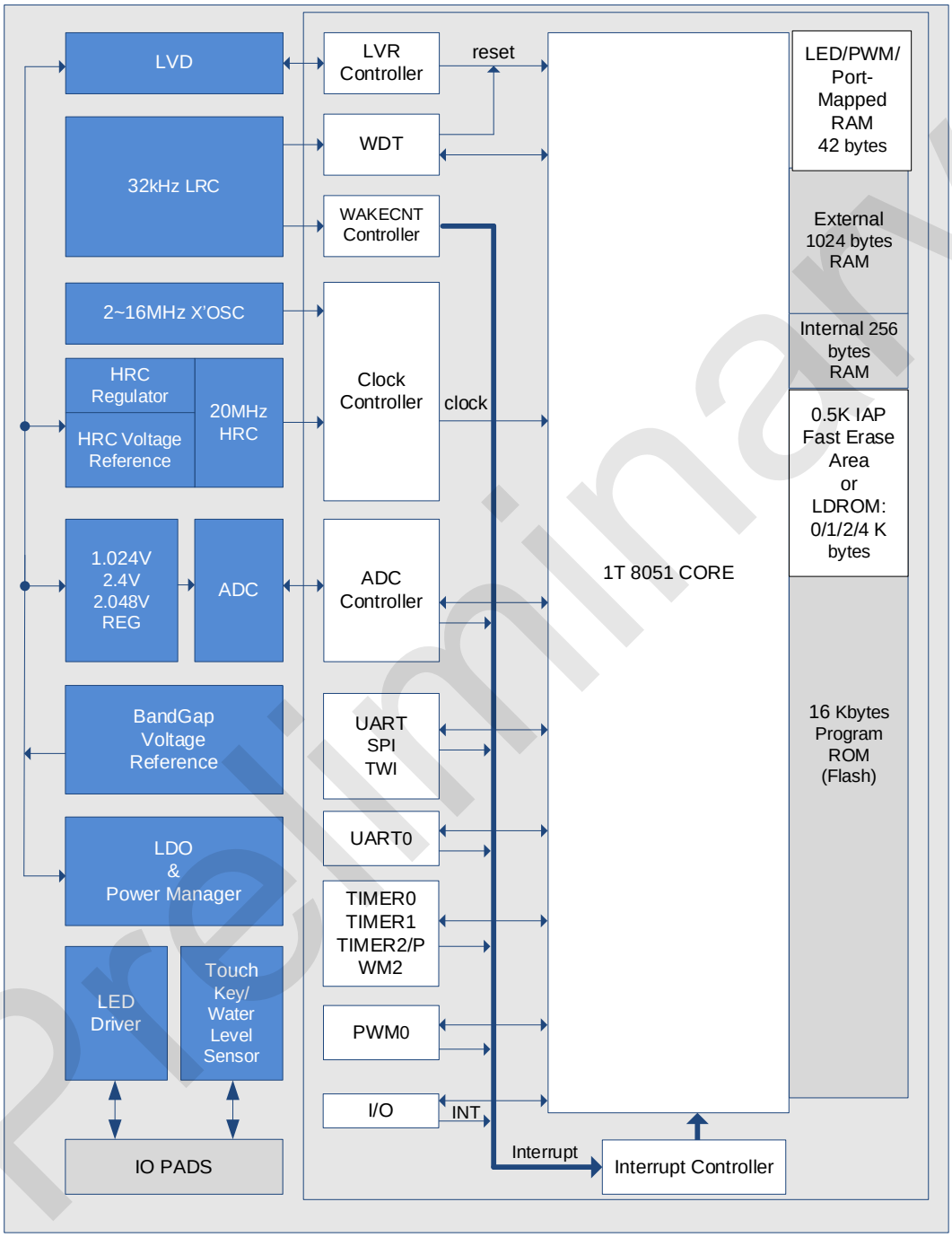
Pin number				Pin name	Pin type	Function description
SOP28/ TSSOP28	SOP20/ TSSOP20	SOP16	SOP8			
				AIN6/TK6/WL6/S9/LED13		T2EX: Timer 2 External Capture Signal Input PWM21: PWM21 output port AIN6: ADC Input Channel 6 TK6: TK channel 6 WL6: WL channel 6 S9: LED normal mode SEG9 LED13: LED drive output port 13
23	**15**	**14**	**-**	**P0.5/INT11/SCL/SCK/FLT/ AIN5/TK5/WL5/S10/LED14**	I/O	P0.5: GPIO P0.5 INT11: External interrupt 1 input 1 SCL: TWI SCL SCK: SPI SCK FLT: PWM0 Fault Detection input pin AIN5: ADC Input Channel 5 TK5: TK channel 5 WL5: WL channel 5 S10: LED normal mode SEG10 LED14: LED drive output port 14
24	**16**	**-**	**-**	**P0.4/INT10/AIN4/TK4/WL4 /S11/LED15**	I/O	P0.4: GPIO P0.4 INT10: External interrupt 1 input 0 AIN4: ADC Input Channel 4 TK4: TK channel 4 WL4: WL channel 4 S11: LED normal mode SEG11 LED15: LED drive output port 15
25	**17**	**-**	**-**	**P0.3/PWM03/AIN3/TK3/W L3**	I/O	P0.3: GPIO P0.3 PWM03: PWM03 output port AIN3: ADC Input Channel 3 TK3: TK channel 3 WL3: WL channel 3
26	**18**	**-**	**-**	**P0.2/PWM02/AIN2/TK2/W L2**	I/O	P0.2: GPIO P0.2 PWM02: PWM02 output port AIN2: ADC Input Channel 2 TK2: TK channel 2 WL2: WL channel 2
27	**19**	**15**	**-**	**P0.1/PWM01/AIN1/TK1/W L1**	I/O	P0.1: GPIO P0.1 PWM01: PWM01 output port AIN1: ADC Input Channel 1 TK1: TK channel 1 WL1: WL channel 1
28	**20**	**16**	**-**	**P0.0/PWM00/AIN0/TK0/W L0**	I/O	P0.0: GPIO P0.0 PWM00: PWM00 output port AIN0: ADC Input Channel 0 TK0: TK channel 0 WL0: WL channel 0

Description:

1. Pins for LED0 to 15 are High Sink Current ports
2. Only LED0 to 11 support bidirectional drive mode

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4 Internal block diagram

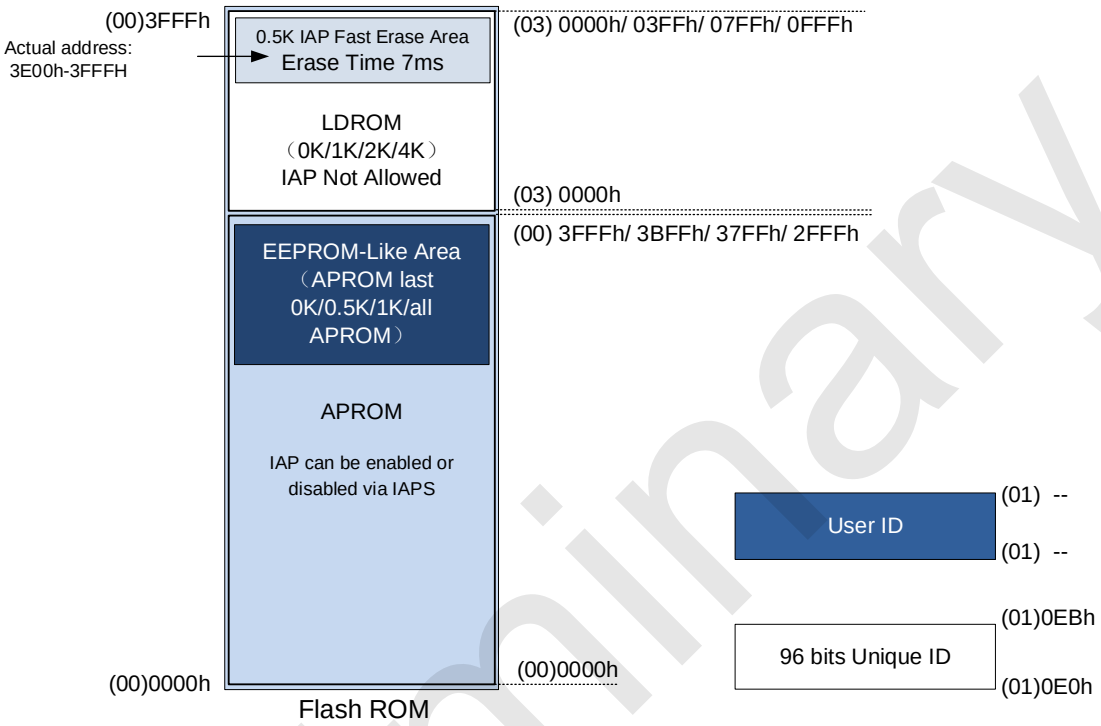


SC92R425B block diagram

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5 Flash ROM and SRAM structure

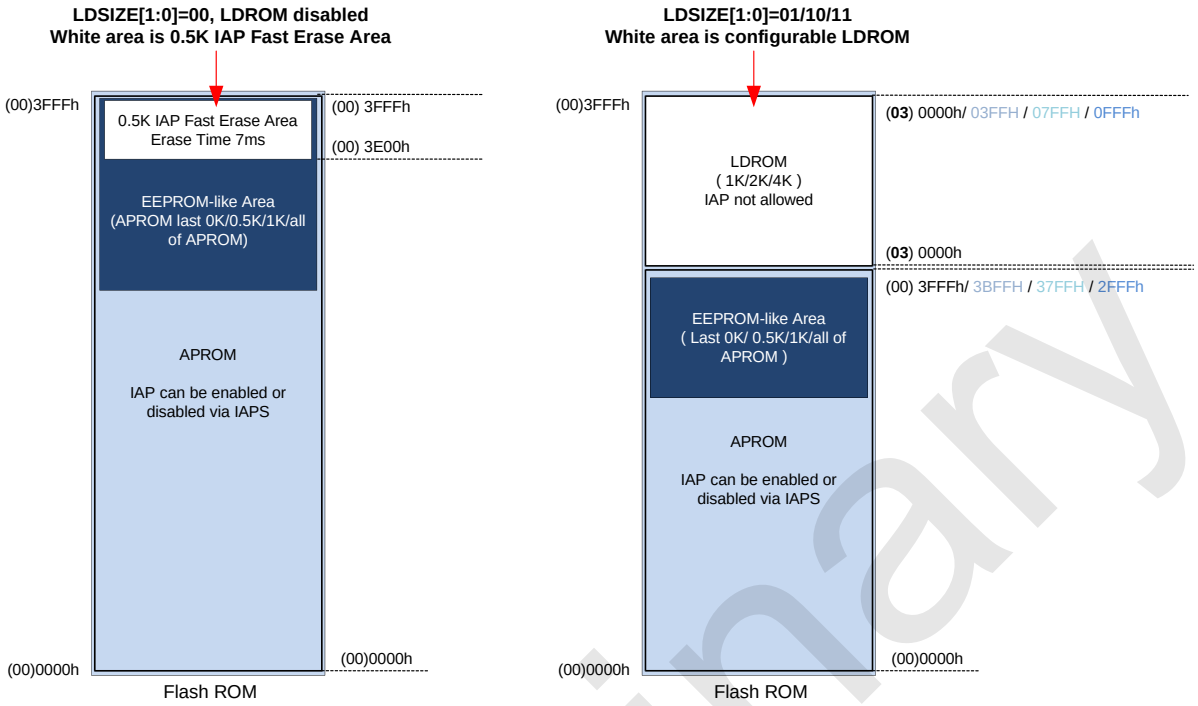
The ROM of the SC92R425B is divided into four areas: APROM / LDROM / User ID / Unique ID. The structure is shown below:



5.1 Structure of the 0.5k IAP fast erase area and LDROM area

The IAP Fast Erase Area and LDROM Area of the SC92R425B share the same physical addresses. The structure is shown below:

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The SC92R425B has a 0.5 Kbytes Fast Erase Area at a fixed address of (00) 3E00H to (00) 3FFFH. When LDSIZE[1:0]=00, meaning the LDROM Area is disabled, the IAP Fast Erase Area is available. Compared with the non-Fast Erase Area, the Fast Erase Area has a shorter erase time of approximately 7 ms.

5.2 APROM and LDROM

APROM and LDROM are two hardware-independent ROM blocks divided by LDSIZE[1:0]. They are distinguished by the Extended Addresses "00" and "03" set through the IAPADE Register, and can be programmed and erased using the dedicated SCLINK PRO Programmer:

- The APROM Area has Extended Address "00" and a selectable size of 12 to 16 Kbytes. It supports IAP (In Application Programming), and the permitted IAP Operation range can be set to 0K / 0.5K / 1K or the entire APROM Area through the Customer Option item
- The LDROM Area has Extended Address "03" and a selectable size of 0 to 4 Kbytes. IAP Operation is not permitted for LDROM.

The SC92R425B has 16 Kbytes of Flash ROM, with addresses from (00)0000H to (00)3FFFH; the "00" in parentheses is the Extended Address, set by the IAPADE Register. Programming and erasing can be performed using SinOne's dedicated ICP Programmer (SC LINK PRO). The 16 Kbytes of Flash ROM has the following features:

- Divided into 128 sectors, each 128 bytes
- Can be written to 10,000 times
- Data can be retained for more than 10 years at an ambient temperature of 25 ℃
- In ICP mode, supports BLANK, PROGRAM, VERIFY, ERASE, and READ functions. The READ function is available only for ICs with the security encryption function disabled
- Security encryption: The APROM (i.e., 16 Kbytes Flash ROM) and LDROM security encryption functions can be enabled or disabled
- IAP (In Application Programming) is supported.

The APROM and LDROM contain a total of 128 sectors, each 128 bytes, and can be written repeatedly up to 10,000 times; at 25°C, data can be retained for more than 10 years.

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SC92R425B APROM sector partition diagram

5.3 96-bit unique ID area

The SC92R425B provides an independent Unique ID Area, in which a 96-bit unique code can be pre-programmed before shipment to ensure the uniqueness of the Chip. The only way for users to obtain the serial number is to read relative addresses (01) 0E0H-0EBH using an IAP Instruction. The "01" in parentheses in addresses (01) 0E0H-0EBH indicates the Extended Address, which is set by the IAPADE Register. The specific operation method is as follows:

IAPADE (F4H) IAP Write Extended Address Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	IAPADER[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7 ~ 0	**IAPADER[7:0]**	IAP extended address: 0x00: MOVC and IAP Programming both target APROM 0x01: Read operations target the **Unique ID** Area; write operations are not allowed 0x02: Reserved 0x03: MOVC targets the LDROM Area (**Note: Only MOVC is allowed; IAP is not allowed. This setting takes effect only when operating on an LDROM program and has no effect when operating on an APROM program**) Other: Reserved

5.3.1 Unique ID read C language example

```
#include "intrins.h"
unsigned char UniqueID [12];//Stores the Unique ID
unsigned char code * POINT =0x0E0
```


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```
unsigned char i

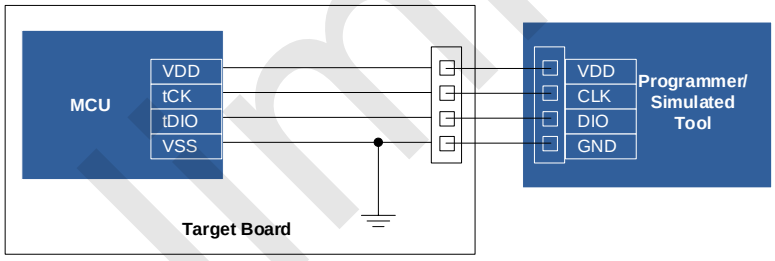

EA = 0; //Disable Global Interrupt
IAPADE = 0x01;//Extended Address 0x01, select the Unique ID Area
for(i=0;i<12;i++)
{
UniqueID [i]= *( POINT+i);//   Read the value of UniqueID
}
IAPADE = 0X00;//Extended Address 0x00, return to Code Area
EA = 1; //Enable Global Interrupt
```

5.4 User ID area

User ID Area, extended Address (01): a user-customized ID is programmed at the factory and can be read by the user, but Write operations to the User ID Area are prohibited.

5.5 Programming

The SC92R425B's APROM and LDROM can be programmed via tDIO, tCK, VDD, and VSS. The specific connections are as follows:



ICP mode programming connection diagram

tDIO and tCK are the signal lines for 2-wire JTAG Flash Programming and debugging. During programming, users can configure the modes of these two Ports through the Customer Option items:

5.5.1 JTAG dedicated mode

tDIO and tCK are dedicated ports for Flash Programming and debugging; other functions multiplexed with them are unavailable. This mode is generally used during online debugging to facilitate debugging. Once JTAG dedicated mode is enabled, the Chip can enter programming or debugging mode directly without being powered off and on again.

5.5.2 Normal mode (JTAG dedicated port disabled)

The JTAG function is unavailable, while other functions multiplexed with it can be used normally. This mode prevents the programming port from occupying MCU Pins, allowing users to make maximum use of MCU resources.

Note: After the configuration to disable the JTAG dedicated port is successfully set, the Chip must be completely powered off and then powered on again before it can enter programming or debugging mode. This affects programming and debugging while the Chip remains powered on. SinOne recommends that users select a configuration that disables the JTAG dedicated port for Mass Programming, and select JTAG mode during the R&D and debugging phase.

The related Customer Option Registers are as follows:

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OP_CTM1 (C2H@FFH)Code Option Register 1 (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	VREFS[1:0]		OP_BL	DISJTG	IAPS[1:0]		LDSIZE[1:0]	
Read/Write	R/W		R/W	R/W	R/W	R/W	R	
Power-On Initial Value	n	n	n	n	n	n	n	n

Bit Number	Bit Symbol	Description
4	DISJTG	IO/JTAG Port Switching Control 0: JTAG mode enabled; P1.2 and P1.3 can only be used as tCK/tDIO. Recommended for development and debugging. 1: Normal mode; JTAG function disabled. Recommended for mass programming.

5.6 IAP (application programming) operation

The IAP area in the SC92R425B APROM (selectable as 0K, 0.5K, 1K, or the entire APROM range) supports IAP (Application Programming) operations. Users can perform remote program updates through IAP operations, or use IAP read operations to obtain information from the Unique ID area or User ID field. Before writing data using IAP, users must erase the Sector containing the target Address. Each Sector is 128 bytes. Flash ROM from (00)0000H to (00)3FFFH is divided into 128 Sectors; the "00" in parentheses is the Extended Address, set by the IAPADE Register:

Note:

1. **During IAP erase/write operations, the CPU holds the Program Counter; only after the IAP erase/write operation is complete does the Program Counter continue executing subsequent instructions.**
2. **The SC92R425B has a 0.5 Kbytes Fast Erase Area, with a fixed address range of (00)3E00H to (00)3FFFH. The IAP Fast Erase Area is available only when LDSIZE[1:0]=00, that is, when the LDROM Area is disabled.**
3. **IAP operations in the APROM Area carry a certain risk. Users must implement appropriate safety measures in software; improper operation may result in the user program being overwritten! Unless this function is necessary (for example, for Remote Program Update), users are advised not to use it.**

Users can select the IAP area range of APROM via Customer Option during programming, and may also configure the IAP area of APROM in the application firmware through the IAPS control bit. The relevant registers are listed below:

OP_CTM1 (C2H@FFH)Customer Option Register 1 (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	VREFS[1:0]		OP_BL	DISJTG	IAPS[1:0]		LDSIZE[1:0]	
Read/Write	R/W		R/W	R/W	R/W	R/W	R	
Power-On Initial Value	n	n	n	n	n	n	n	n

Bit Number	Bit Symbol	Description
3 ~ 2	IAPS[1:0]	IAP Space Range Selection 00: IAP operation is not allowed in any Flash ROM 01: IAP operation is allowed in the last 0.5K of Flash ROM 10: IAP operation is allowed in the last 1K of Flash ROM

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Bit Number	Bit Symbol	Description
		11: IAP operation is allowed in all Flash ROM **Note:** **1. The above settings are invalid in BootLoader mode. The BootLoader program can perform IAP operations on the entire APROM Area.** **2. IAP operation is not allowed in LDROM under any circumstances**

5.6.1 Registers related to IAP operation

Description of Registers Related to IAP Operation:

Symbol	Address	Description	7	6	5	4	3	2	1	0	Reset value
IAPKEY	F1H	Data Protection Register	IAPKEY[7:0]								00000000b
IAPADL	F2H	IAP Write Address Low Byte Register	IAPADR[7:0]								00000000b
IAPADH	F3H	IAP Write Address High Byte Register	-	-	IAPADR[13:8]						xx000000b
IAPADE	F4H	IAP Write Extended Address Register	IAPADER[7:0]								00000000b
IAPDAT	F5H	IAP Data Register	IAPDAT[7:0]								00000000b
IAPCTL	F6H	IAP Control Register	BTLD	ERASE	PERASE	SERASE	PRG	-	CMD[1:0]		00000x00b

IAPKEY (F1H)IAP Protection Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	IAPKEY[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7 ~ 0	IAPKEY[7:0]	Enable the IAP function and set the operation time limit Write a value n greater than or equal to 0x40, which means: ● Enable the IAP function ● If no Write command is received within n System Clocks, the IAP function will be automatically disabled.

IAPADL (F2H)IAP Write Address Low Byte Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	IAPADR[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7 ~ 0	IAPADR[7:0]	Lower 8 Bits of the IAP write address

IAPADH (F3H)IAP Write Address High Byte Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	-	-	IAPADR[13:8]					

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Bit Number	7	6	5	4	3	2	1	0
Read/Write	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	x	x	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
5 ~ 0	IAPADR[13:8]	Upper 6 bits of the IAP write address
7 ~ 6	-	Reserved

IAPADE (F4H) IAP Write Extended Address Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	IAPADER[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7 ~ 0	IAPADER[7:0]	IAP extended address: 0x00: MOVC and IAP Programming both target APROM **0x01: Read operation for the Unique ID Area; writing is not allowed!** 0x02: Reserved 0x03: MOVC targets the LDROM Area (**Note: Only MOVC is allowed; IAP is not allowed. This setting takes effect only when operating on an LDROM program and has no effect when operating on an APROM program**) Other: Reserved

IAPDAT (F5H)IAP Data Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	IAPDAT[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7 ~ 0	IAPDAT	IAPDAT[7:0] is the data to be written by IAP

IAPCTL (F6H) IAP Control Register

Bit Number	7	6	5	4	3	2	1	0
Symbol	BTLD	ERASE	PERASE	SERASE	PRG	-	CMD[1:0]	
Read/Write	R/W	R/W	R/W	R/W	R/W	-	R/W	R/W
Power-On Initial Value	0	0	0	0	0	x	0	0

Bit Number	Bit Symbol	Description
7	BTLD	BootLoader Control Bit

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Bit Number	Bit Symbol	Description
		0: After a Software reset, the program starts running from the Main program area (main program) 1: After a Software reset, the program starts running from the BootLoader area
6	ERASE	Chip Erase Control Bit 0: No operation 1: After setting to "1", then configuring CMD[1:0]=10, the APROM Chip Erase operation is entered, and all of APROM will be erased Note: When the LDROM protection lock is not enabled (LDLOCK=0), performing Chip Erase will erase both APROM and LDROM! To ensure that only APROM is erased without affecting LDROM when performing an IAP update in LDROM, be sure to enable the LDROM protection lock (LDLOCK=1) before invoking the Chip Erase function.
5	PERASE	Page Erase Control Bit 0: No operation 1: Set to "1" and then configure CMD[1:0]=10 to initiate a Flash ROM Page Erase operation; the specified Page (1024 bytes) of Flash ROM will be erased
4	SERASE	Sector Erase Control Bit 0: No operation 1: Set to "1" and then configure CMD[1:0]=10 to initiate a Flash ROM Sector Erase operation; the specified Sector of Flash ROM will be erased
3	PRG	Program Control Bit 0: No operation 1: Set to "1" and then configure CMD[1:0]=10 to initiate a Flash ROM Write operation; the Data in the IAPDAT Register will be written to the specified Flash ROM Address
1 ~ 0	CMD[1:0]	IAP command enable control bits 10: Execute the Write or Sector Erase command Other: Reserved **Note:** ● **After setting SERASE / PRG to "1", CMD[1:0]=10 must be configured for the corresponding operation to begin** ● **Only one type of IAP Operation can be performed at a time; therefore, only one of the SERASE or PRG bits can be set to "1" simultaneously** ● **At least 8 NOP instructions must be added after the IAP Operation statement to ensure that subsequent instructions execute normally after the IAP Operation is completed**
2	-	Reserved

PCON (87H) Power Management Control Register (W, *not readable *)

Bit Number	7	6	5	4	3	2	1	0
Symbol	SMOD	-	LDLOCK	-	RST	-	STOP	IDL
Read/Write	W	-	W	-	W	-	W	W
Power-On Initial Value	0	x	0	x	n	x	0	0

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Bit Number	Bit Symbol	Description
5	**LDLOCK**	**LDROM Protection Lock** 0: LDROM is not protected 1: Enable LDROM hardware protection logic. This allows users to quickly erase APROM with the Chip Erase command when updating the program through IAP Operation, without affecting LDROM.

5.6.2 IAP operation flow

For the SC92R425B IAP Operation Flow, refer to the "SC92R425B IAP Operation Library Package."

5.6.3 IAP operation precautions

1. When programming the IC, if "Disable IAP operation in APROM area" is selected via Code Option, then when IAPADE[7:0]=0x00 (APROM Area selected), IAP cannot be performed; that is, Data cannot be written, and Data can only be read using the MOVC Instruction.
2. When IAPADE is not 0x00, MOVC and Write operations target a non-APROM Area. If an Interrupt occurs at this time and an MOVC operation is performed in the Interrupt routine, the MOVC result will be incorrect, causing abnormal program execution. To prevent this, during IAP Operation, if IAPADE is not 0x00, be sure to disable Global Interrupts (EA=0) before the operation, then set IAPADE =0X00 after the operation is complete before enabling Global Interrupts (EA=1).
3. During IAP erase/write operations, the CPU holds the Program Counter; the Program Counter resumes execution of subsequent instructions only after the IAP erase/write operation is complete.
4. IAP operations within the APROM Area carry some risk. Users must implement appropriate safeguards in their software; improper operation may overwrite the user program. Unless this function is essential (for example, for Remote Program Update), its use is not recommended.

5.6.4 IAP operation C language example

The following examples share the header file below:

```
#include "intrins.h"
unsigned int IAP_Add
unsigned char IAP_Data
unsigned char code * POINT =0x00
```

5.6.4.1 IAP operation: read data

```
EA = 0;//Disable Global Interrupt
IAPADE = 0X00;//Extended Address is 0x00; select APROM
IAP_Data = *( POINT+IAP_Add);//Read the value at IAP_Add into IAP_Data
EA = 1;//Enable Global Interrupt
```

5.6.4.2 IAP operation: Erase/Write

For IAP erase/write operations, users should refer to the SC92R425B IAP Operation Library Package

5.7 Bootloader function

LDROM is used to store the IC's BootLoader boot code. In ICP mode, LDROM supports Blank Check (BLANK), Programming (PROGRAM), Verification (VERIFY), Erase (ERASE), and Read (READ). Users can also download their own boot code to LDROM using a Programmer.

Users can implement ISP (In System Programming) using LDROM: during ISP execution, the IC runs the boot code in the LDROM area. While the boot code is running, it receives new program code through the Serial

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Port, then programs the received code into the user code area using an IAP command. The entire process does not require removing the chip from the system board or using a Programmer.

Four LDROM address range options are available:

- (03) 0000H to (03)0000H (LDROM disabled)
- (03) 0000H to (03)03FFH (1K)
- (03) 0000H to (03)07FFH (2K)
- (03) 0000H to (03)0FFFH (4K)

Here, "03" in parentheses in the addresses above indicates the Extended Address, set by LDSIZE[1:0].

5.7.1 Registers related to BootLoader mode operations

OP_CTM1 (C2H@FFH)Code Option Register 1 (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	VREFS[1:0]		OP_BL	DISJTG	IAPS[1:0]		LDSIZE[1:0]	
Read/Write	R/W		R/W	R/W	R/W	R/W	R	
Power-On Initial Value	n	n	n	n	n	n	n	n

Bit Number	Bit Symbol	Description
5	OP_BL	Program Execution Area Control Bit 0: Enter APROM after chip reset 1: Enter LDROM after chip reset 1. The restrictions on MOVC and IAP operations in APROM are as follows: Operation / Allowed MOVC to LDROM / x MOVC to APROM / √ IAP to LDROM / × IAP to APROM / √ 2. The restrictions on MOVC and IAP operations in LDROM are as follows: Operation / Allowed MOVC to LDROM / √ MOVC to APROM / √ IAP to LDROM / × IAP to the entire APROM is not restricted by IAPRANGE / √
1 ~ 0	LDSIZE[1:0]	LDROM Space Range Selection 00: LDROM disabled, APROM Address 0000H to 3FFFH 01: The last 1K of Flash ROM is the LDROM Area; APROM Address 0000H to 3BFFH 10: The last 2K of Flash ROM is the LDROM Area; APROM Address 0000H to 37FFH

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Bit Number	Bit Symbol	Description
		11: The last 4K of Flash ROM is the LDROM Area; APROM Address 0000H to 2FFFH **Note: IAP operations on LDROM are prohibited under any circumstances**

IAPKEY (F1H) Data Protection Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	IAPKEY[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7 ~ 0	IAPKEY[7:0]	Enable the IAP function and set the operation time limit Write a value n greater than or equal to 0x40, which means: ● Enable the IAP function ● If no IAP Write command is received within n System Clocks, the IAP function will be automatically disabled.

IAPADL (F2H)IAP Write Address Low Byte Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	IAPADR[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7 ~ 0	IAPADR[7:0]	Lower 8 Bits of the IAP write address

IAPADH (F3H)IAP Write Address High Byte Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	-	-	IAPADR[13:8]					
Read/Write	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	x	x	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
5 ~ 0	IAPADR[13:8]	Upper 6 bits of the IAP write address

IAPADE (F4H) IAP Write Extended Address Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	IAPADER[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

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Bit Number	7	6	5	4	3	2	1	0
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7 ~ 0	IAPADER[7:0]	IAP extended address: 0x00: MOVC and IAP Programming both target APROM 0x01: Read operations are permitted for the Unique ID Area; Write operations are not permitted 0x02: Reserved 0x03: MOVC targets the LDROM Area (**Note: Only MOVC is allowed; IAP is not allowed. This setting takes effect only when operating on an LDROM program and has no effect when operating on an APROM program**) Other: Reserved

IAPDAT (F5H)IAP Data Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	IAPDAT[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7 ~ 0	IAPDAT[7:0]	Data written by IAP

IAPCTL (F6H) IAP Control Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	BTLD	ERASE	PERASE	SERASE	PRG	-	CMD[1:0]	
Read/Write	R/W	R/W	R/W	R/W	R/W	-	R/W	R/W
Power-On Initial Value	0	0	0	0	0	x	0	0

Bit Number	Bit Symbol	Description
7	BTLD	BootLoader Control Bit 0: After a Software reset, the program starts running from the Main program area (main program) 1: After a Software reset, the program starts running from the BootLoader area

PCON (87h) Power Management Control Register (W only, *not readable *)

Bit Number	7	6	5	4	3	2	1	0
Symbol	SMOD	-	LDLOCK	-	RST	-	STOP	IDL
Read/Write	W	-	W	-	W	-	W	W

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Bit Number	7	6	5	4	3	2	1	0
Power-On Initial Value	0	x	0	x	n	x	0	0

Bit Number	Bit Symbol	Description
3	RST	Software Reset Control Bit: Write status: 0: Program runs normally 1: The CPU resets immediately after this bit is written to "1"

BootLoader operation notes:

1. **Before writing data to the Code Area, the user must erase the sector containing the target address.**
2. **For details on how to perform this operation, refer to SinOne's document 《SinOne Hardware BootLoader Function Implementation Application Guide》.**

5.8 Security encryption

Users can select whether to enable the SC92R425B ROM security encryption function using the "Encryption" setting in the Programming Host Software interface:

1. When the security encryption function is disabled, users can read the data in APROM (i.e., 16 Kbytes of Flash ROM) and LDROM using a Programmer, which facilitates development and debugging
2. When secure encryption is enabled, the data in APROM and LDROM cannot be read externally. When a user performs a reprogramming operation on an SC92R425B with the encryption function enabled using a Programmer, regardless of whether the target is APROM or LDROM, the Programmer first forcibly erases both APROM and LDROM before performing the Write operation. Users are advised to enable the security encryption function for Mass Programming
3. The only way to disable security encryption is to turn off the security encryption function and perform a Programming operation
4. Security encryption does not affect the IAP function

For specific procedures, see the Security Encryption and Read chapters of the Programming Tool User Manual.

5.9 Customer option area (user programming settings)

The SC92R425B has a separate Flash Area for storing the user's Power-On Initial Value settings. This Area is called the Code Option Area. When Programming the IC, the user writes this code to the IC's internal memory. During Reset initialization, the IC loads these settings into the SFRs as initial values.

Option-related SFR operation description:

Read and Write operations for Option-related SFRs are controlled by the OPINX and OPREG Registers. The specific locations of the Option SFRs are determined by OPINX, as shown in the following table:

Symbol	Address	Description	7	6	5	4	3	2	1	0
OP_CTM0	C1H@FFH	Customer Option Register 0	ENWDT	ENXTL	SCLKS[1:0]		DISRST	DISLVR	LVRS[1:0]	
OP_CTM1	C2H@FFH	Customer Option Register 1	VREFS[1:0]		OP_BL	DISJTG	IAPS[1:0]		LDSIZE[1:0]	
OP_HRCR	83H@FFH	System Clock Change Register	-	-	OP_HRCR[5:0]					

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<table>
<tr><th>IFB Address</th><th>Symbol</th><th>Read/Write</th><th>Description</th></tr>
<tr><td>OP_CTM0[7]</td><td>ENWDT</td><td>R/W</td><td>WDT Enable/Disable
0: WDT disabled
1: WDT enabled (but the WDT stops counting while the IC is executing IAP)</td></tr>
<tr><td>OP_CTM0[6]</td><td>ENXTL</td><td>R/W</td><td>External Crystal Oscillator Selection
0: External Crystal Oscillator off; P5.0 and P5.1 enabled
1: External Crystal Oscillator on; P5.0 and P5.1 disabled.</td></tr>
<tr><td>OP_CTM0
[5 ~ 4]</td><td>SCLKS[1:0]</td><td>R/W</td><td>System Clock Frequency selection:
00: System Clock Frequency is the High-frequency oscillator frequency divided by 1
01: System Clock Frequency is the High-frequency oscillator frequency divided by 2
10: System Clock Frequency is the High-frequency oscillator frequency divided by 4
11: System Clock Frequency is the High-frequency oscillator frequency divided by 12.</td></tr>
<tr><td>OP_CTM0[3]</td><td>DISRST</td><td>R</td><td>IO/RST switching control
0: P1.1 used as the Reset Pin
1: P1.1 used as a normal I/O Pin</td></tr>
<tr><td>OP_CTM0[2]</td><td>DISLVR</td><td>R/W</td><td>LVR Enable
0: LVR enabled
1: LVR disabled</td></tr>
<tr><td>OP_CTM0
[1 ~ 0]</td><td>LVRS [1:0]</td><td>R/W</td><td>LVR Voltage Selection Control
11: 4.3 V Reset
10: 3.7 V Reset
01: 2.9 V Reset
00: 2.3 V Reset</td></tr>
<tr><td>OP_CTM1[7 ~ 6]</td><td>VREFS[1:0]</td><td>R/W</td><td>Reference Voltage Selection (initial value loaded from Code Option; user-configurable)
00: Set the ADC V_{REF} to V_{DD}
01: Set the ADC V_{REF} to the precise internal 1.024 V
10: Set the ADC V_{REF} to the precise internal 2.4 V
11: Set the ADC V_{REF} to the precise internal 2.048 V.</td></tr>
<tr><td>OP_CTM1[5]</td><td>OP_BL</td><td>R/W</td><td>Program Execution Area Control Bit
0: Enter APROM after chip reset
1: Enter LDROM after chip reset

The restrictions on MOVC and IAP operations in APROM are as follows:
<table>
<tr><th>Operation</th><th>Allowed</th></tr>
<tr><td>MOVC to LDROM</td><td>x</td></tr>
<tr><td>MOVC to APROM</td><td>√</td></tr>
<tr><td>IAP to LDROM</td><td>×</td></tr>
<tr><td>IAP to APROM</td><td>√</td></tr>
</table>
The restrictions on MOVC and IAP operations in LDROM are as follows:
<table>
<tr><th>Operation</th><th>Allowed</th></tr>
<tr><td>MOVC to LDROM</td><td>√</td></tr>
<tr><td>MOVC to APROM</td><td>√</td></tr>
<tr><td>IAP to LDROM</td><td>×</td></tr>
<tr><td>IAP to the entire APROM is not restricted by IAPRANGE</td><td>√</td></tr>
</table></td></tr>
<tr><td>OP_CTM1[4]</td><td>DISJTG</td><td>R/W</td><td>IO/JTAG Port Switching Control
0: JTAG mode enabled; P1.2 and P1.3 can only be used as tCK/tDIO
1: Normal mode (Normal); JTAG function disabled</td></tr>
<tr><td>OP_CTM1
[3 ~ 2]</td><td>IAPS[1:0]</td><td>R/W</td><td>IAP Space Range Selection
00: IAP Operation prohibited in the Code Area
01: IAP Operation allowed in the last 0.5K of the Code Area
10: IAP Operation allowed in the last 1K of the Code Area
11: IAP Operation allowed in the entire Code Area
Note:
1. The above settings are invalid in BootLoader mode. The BootLoader program can perform IAP Operation on the entire APROM Area.
2. IAP Operation is not allowed in LDROM under any circumstances.</td></tr>
</table>

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<table>
<tr><th>IFB Address</th><th>Symbol</th><th>Read/Write</th><th>Description</th></tr>
<tr><td>OP_CTM1[1:0]</td><td>LDSIZE[1:0]</td><td>R</td><td>LDROM Space Range Selection
00: LDROM disabled, APROM Address 0000H to 3FFFH
01: The last 1K of Flash ROM is the LDROM Area; APROM Address 0000H to 3BFFH
10: The last 2K of Flash ROM is the LDROM Area; APROM Address 0000H to 37FFH
11: The last 4K of Flash ROM is the LDROM Area; APROM Address 0000H to 2FFFH
Note: IAP operations on LDROM are prohibited under any circumstances.</td></tr>
<tr><td>OP_HRCR</td><td>OP_HRCR[5:0]</td><td>R/W</td><td>HRC frequency adjustment register
Users can change the high-frequency oscillator frequency f_{HRC} by modifying the value of this Register, thereby changing the IC's System Clock Frequency f_{SYS}:
1. The initial power-on value OP_HRCR[s] of OP_HRCR[5:0] is fixed to ensure that f_{HRC} is 20 MHz; OP_HRCR[s] may vary from one IC to another
2. When the initial value is OP_HRCR[s], the IC's System Clock Frequency f_{SYS} can be set to an accurate 10/5/1.66 MHz using the Option item; each change of 1 in OP_HRCR [5:0] changes the f_{SYS}
The relationship between the OP_HRCR [5:0] value and the f_{SYS} output Frequency is as follows:
<table>
<tr><td>OP_HRCR [5:0] value</td><td>f_{SYS} Actual output frequency (10M as an example)</td></tr>
<tr><td>OP_HRCR [s]-n</td><td>10000*(1-0.5%*n)kHz</td></tr>
<tr><td>...</td><td>....</td></tr>
<tr><td>OP_HRCR [s]-2</td><td>10000*(1-0.5%*2) = 9900kHz</td></tr>
<tr><td>OP_HRCR [s]-1</td><td>10000*(1-0.5%*1) = 9950kHz</td></tr>
<tr><td>OP_HRCR [s]</td><td>10000kHz</td></tr>
<tr><td>OP_HRCR [s]+1</td><td>10000*(1+0.5%*1) = 10050kHz</td></tr>
<tr><td>OP_HRCR [s]+2</td><td>10000*(1+0.5%*2) = 10100kHz</td></tr>
<tr><td>...</td><td>...</td></tr>
<tr><td>OP_HRCR [s]+n</td><td>10000*(1+0.5%*n)kHz</td></tr>
</table>
Note:
1. After each Power-on, the value of OP_HRCR[5:0] is the value closest to 20 MHz for the High-frequency oscillator frequency f_{HRC}.
2. To ensure reliable IC operation, the IC's maximum operating frequency should preferably not exceed 110% of 10 MHz, i.e., 11 MHz.
3. Please confirm that changing the HRC Frequency will not affect other functions.</td></tr>
</table>

5.9.1 Option-related SFR operation description

Read and write operations for Option-related SFRs are controlled by the OPINX and OPREG registers. The specific location of each Option SFR is determined by OPINX, and the value written to each Option SFR is determined by OPREG:

Symbol	Address	Description	7	6	5	4	3	2	1	0	Power-On Initial Value
OPINX	FEH	Option Pointer	OPINX[7:0]								00000000b
OPREG	FFH	Option Register	OPREG[7:0]								nnnnnnnnb

When operating on Option-related SFRs, the OPINX register stores the address of the relevant OPTION register, and the OPREG register stores the corresponding value.

For example, to configure OP_HRCR to 0x01, proceed as follows:

C Language Example:

OPINX = 0x83;//Write the address of OP_HRCR to the OPINX register

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OPREG = 0x01;//Write 0x01 to the OPREG register (the value to be written to the OP_HRCR register)

Assembly routine:

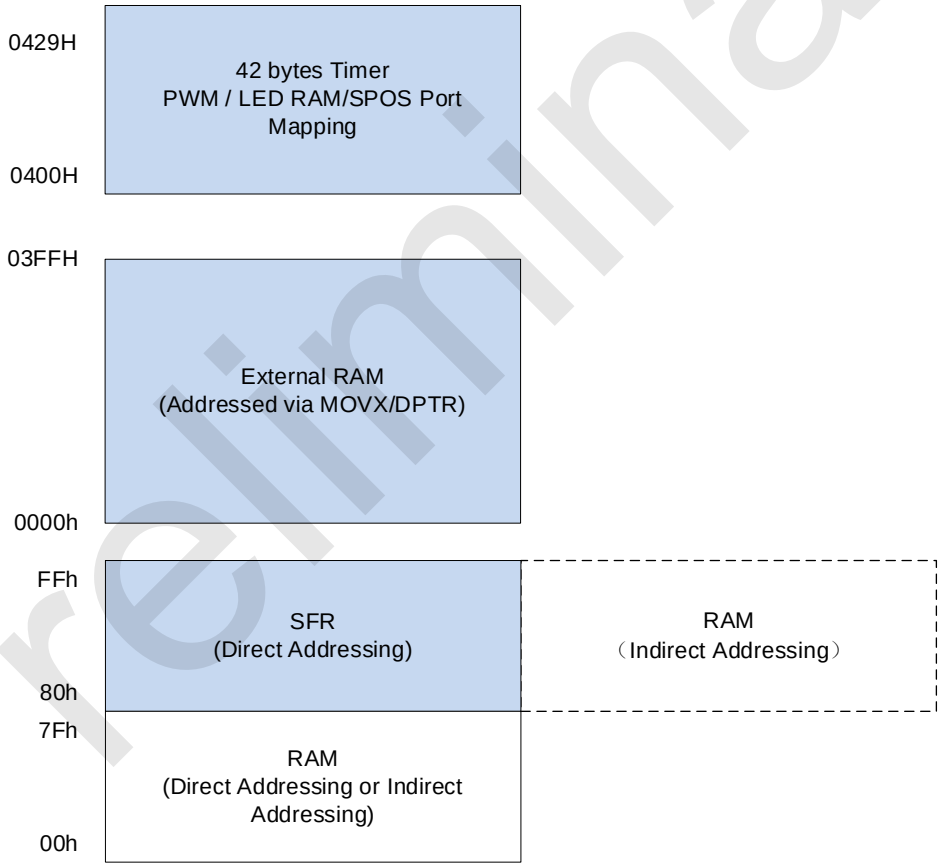
MOV OPINX,#83H; Write the address of OP_HRCR to the OPINX Register

MOV OPREG,#01H; Write 0x01 (the value to be written to the OP_HRCR Register) to the OPREG Register

Note: Do not write any value other than a Customer Option Area SFR address to the OPINX Register! Otherwise, the system may operate abnormally!

5.10 SRAM

The SRAM structure of the SC92R425B is as follows:



The SC92R425B microcontroller integrates 1.25 Kbytes of SRAM, comprising Internal 256 bytes RAM and External 1024 bytes RAM. The address range of the internal RAM is 00H to FFH. The Upper 128 bytes (addresses 80H to FFH) can only be accessed indirectly, while the Lower 128 bytes (addresses 00H to 7FH) can be accessed directly or indirectly.

The address range of the Special Function Register (SFR) is also 80H to FFH. However, the difference between SFR Registers and the Upper 128 bytes of internal SRAM is that SFR Registers use Direct Addressing, while the Upper 128 bytes of internal SRAM can only be accessed by Indirect Addressing.

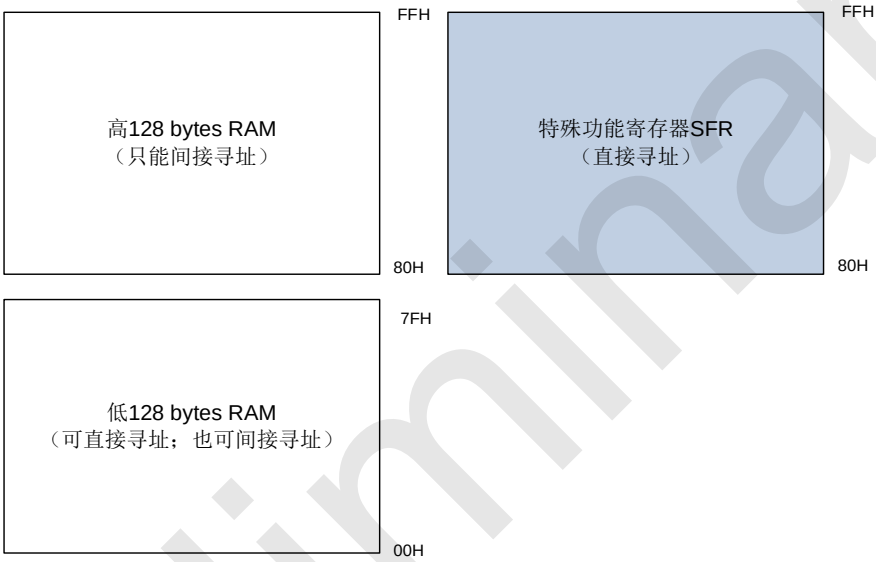
The External RAM address range is 0000H to 03FFH, but it must be addressed using the MOVX instruction.

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42 bytes of PWM/LED RAM; see 42-byte Register Extended RAM for details.

5.10.1 Internal 256 bytes SRAM

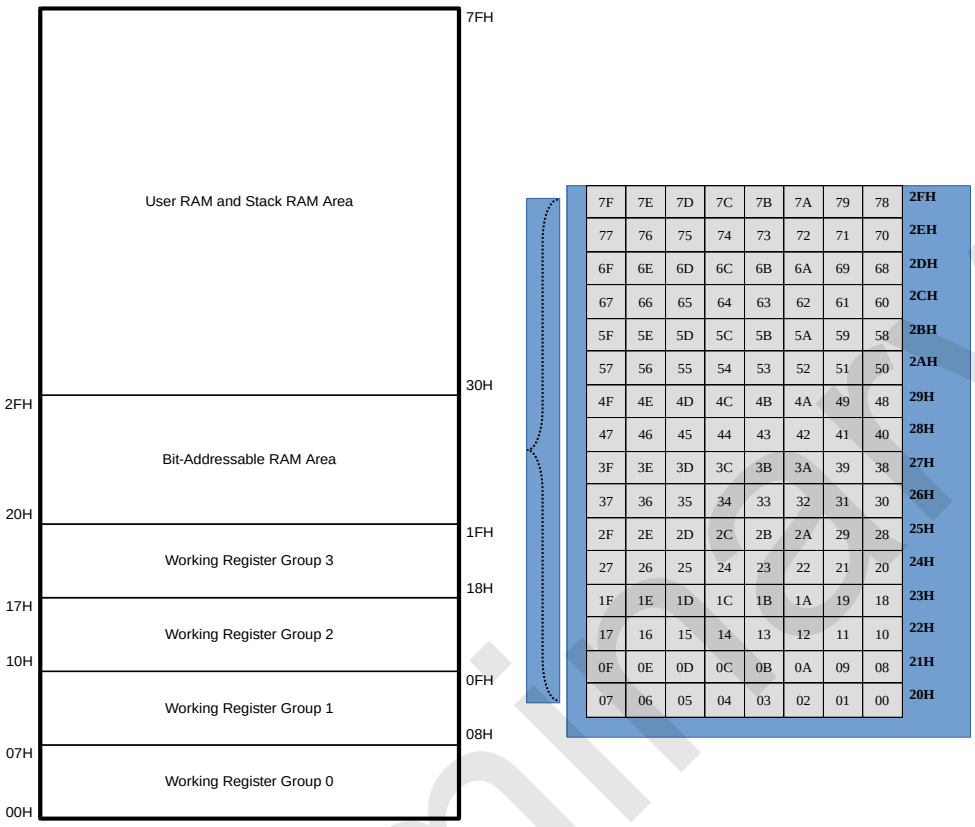
The internal lower 128 bytes SRAM area can be divided into three parts: ① Working Register Groups 0-3, addresses 00H-1FH. The RS0 and RS1 bits in the Program Status Word Register (PSW) determine the Working Register Group currently in use. Using Working Register Groups 0-3 can speed up calculations; ② Bit-addressable area 20H-2FH. This area can be used as ordinary RAM or as bit-addressable RAM; For bit addressing, bit addresses range from 00H to 7FH (these addresses are assigned by bit, unlike general-purpose SRAM addresses, which are assigned by byte), and can be distinguished by instructions in the program; ③ User RAM and Stack area. After the SC92R425B is reset, the 8-bit Stack pointer points to the Stack area. Users generally set its initial value in the initialization routine; it is recommended to set it within the address range E0H-FFH.



Internal 256 bytes RAM structure diagram

The lower 128 bytes of internal RAM are structured as follows:

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SRAM structure diagram

5.10.2 External 1024-byte SRAM

The external 1024-byte RAM can be accessed using MOVX @DPTR, A; The external 1024-byte RAM can also be accessed using MOVX A, @Ri or MOVX @Ri, A in conjunction with the EXADH Register: the EXADH Register stores the Most Significant Bit of the external SRAM Address, and the Ri Register stores the Lower 8 Bits of the external SRAM Address.

EXADH (F7H) External SRAM operation Address high byte (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	EXADH [1:0]	
Power-On Initial Value	x	x	x	x	x	x	0	0

Bit Number	Bit Symbol	Description
1 ~ 0	**EXADH [1:0]**	High bit of the external SRAM operation Address
7 ~ 2	**-**	Reserved

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6 Special function register (SFR)

6.1 SFR mapping

The SC92R425B series has a number of special function registers, known as SFRs. The addresses of these SFRs are in the range 80H-FFH; some are bit-addressable and some are not. The addresses of bit-addressable registers always end in "0" or "8". These registers are very convenient when you need to change the value of a single bit. All SFRs must be accessed using direct addressing.

The names and addresses of the SC92R425B special function registers are listed in the following table:

	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
F8h	-	-	-	-	CRCINX	CRCREG	OPINX	OPREG
F0h	B	IAPKEY	IAPADL	IAPADH	IAPADE	IAPDAT	IAPCTL	EXADH
E8h	-	EXA0	EXA1	EXA2	EXA3	EXBL	EXBH	OPERCON
E0h	ACC	-	-	-	-	-	-	-
D8h	P5	P5CON	P5PH	-	-	-	-	-
D0h	PSW	PWMCFG	PWMCON0	PWMCON1	PWMPDL	PWMPDH	PWMDFR	PWMFLT
C8h	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2	BTMCON	WDTCON
C0h	-	-	-	-	-	-	-	-
B8h	IP	IP1	INT0F	INT0R	INT1F	INT1R	-	-
B0h	-	-	-	-				
A8h	IE	IE1	ADCCFG2	ADCCFG0	-	ADCCON	ADCVL	ADCVH
A0h	P2	P2CON	P2PH	-	-	-	-	-
98h	SCON	SBUF	P0CON	P0PH	LEDVO0	SSCON0	SSCON1	SSDAT
90h	P1	P1CON	P1PH	LEDVO1	-	SSCON2	DDRCON	SCANCON
88h	TCON	TMOD	TL0	TL1	TH0	TH1	TMCON	OTCON
80h	P0	SP	DPL	DPH	-	-	-	PCON
			Bit-addressable			Not bit-addressable		

Description:

1. Empty cells in the SFR map indicate reserved addresses, users are not recommended to access them.
2. F1H to FFH in the SFR are Special Function Registers used for system configuration. User's modification may cause system errors. Users must not modify these registers during system initialization.

6.2 SFR description

The detailed descriptions of the Special Function Registers (SFRs) are as follows:

Symbol	Address	Description	7	6	5	4	3	2	1	0	Power-On Initial Value
P0	80H	Port P0 Data Register	P07	P06	P05	P04	P03	P02	P01	P00	00000000b
SP	81H	Stack pointer	SP[7:0]								00000111b
DPL	82H	DPTR Data Pointer Low-order bit	DPL[7:0]								00000000b
DPH	83H	DPTR Data Pointer Most Significant Bit	DPH[7:0]								00000000b
PCON	87H	Power Management Control Register	SMOD	-	LDLOCK	-	RST	-	STOP	IDL	0x0x0x00b

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Symbol	Address	Description	7	6	5	4	3	2	1	0	Power-On Initial Value
TCON	88H	Timer Control Register	TF1	TR1	TF0	TR0	IE1	-	IE0	-	00000x0xb
TMOD	89H	Timer Working Mode Register	-	C/T1	M11	M01	-	C/T0	M10	M00	x000x000b
TL0	8AH	Timer 0 Lower 8 Bits	TL0[7:0]								00000000b
TL1	8BH	Timer 1 Lower 8 Bits	TL1[7:0]								00000000b
TH0	8CH	Timer 0 High 8 Bits	TH0[7:0]								00000000b
TH1	8DH	Timer 1 High 8 Bits	TH1[7:0]								00000000b
TMCON	8EH	Timer Frequency Control Register	-	-	-	-	-	-	T1FD	T0FD	xxxxxx00b
OTCON	8FH	Output Control Register	SSMOD[1:0]				-	-	-	-	00xxxxxxb
P1	90H	P1 Port Data Register	P17	P16	P15	P14	P13	P12	P11	P10	00000000b
P1CON	91H	P1 Port Input/Output Control Register	P1C7	P1C6	P1C5	P1C4	P1C3	P1C2	P1C1	P1C0	00000000b
P1PH	92H	P1 Port Pull-Up Resistor Control Register	P1H7	P1H6	P1H5	P1H4	P1H3	P1H2	P1H1	P1H0	00000000b
LEDVO1	93H	LED Display Driver Output Register 1	LED15VO	LED14VO	LED13VO	LED12VO	LED11VO	LED10VO	LED9VO	LED8VO	00000000b
SSCON2	95H	SSI control register 2	SSCON2[7:0]								00000000b
DDRCON	96H	Display driver control register	DDRON	DMOD	DUTY[1:0]		DRIV[3:0]				00001111b
SCANCON	97H	Display driver scan configuration register	AUIF	CMEN	LEDXT[1:0]		LTSEL[1:0]		LEDCK[1:0]		00010000b
SCON	98H	Serial Port Control Register	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	00000000b
SBUF	99H	Serial Port Data Buffer Register	SBUF[7:0]								00000000b
P0CON	9AH	P0 Port Input/Output Control Register	P0C7	P0C6	P0C5	P0C4	P0C3	P0C2	P0C1	P0C0	00000000b
P0PH	9BH	P0 Port Pull-Up Resistor Control Register	P0H7	P0H6	P0H5	P0H4	P0H3	P0H2	P0H1	P0H0	00000000b
LEDVO0	9CH	LED Display Driver Output Register 0	LED7VO	LED6VO	LED5VO	LED4VO	LED3VO	LED2VO	LED1VO	LED0VO	00000000b
SSCON0	9DH	SSI control register 0	SSCON0[7:0]								00000000b
SSCON1	9EH	SSI control register 1	SSCON1[7:0]								00000000b
SSDAT	9FH	SSI Data Register	SSD[7:0]								00000000b
P2	A0H	Port P2 Data Register	P27	P26	P25	P24	P23	P22	P21	P20	00000000b
P2CON	A1H	P2 Port Input/Output Control Register	P2C7	P2C6	P2C5	P2C4	P2C3	P2C2	P2C1	P2C0	00000000b
P2PH	A2H	P2 Port Pull-Up Resistor Control Register	P2H7	P2H6	P2H5	P2H4	P2H3	P2H2	P2H1	P2H0	00000000b
IE	A8H	Interrupt Enable Register	EA	EADC	ET2	EUART	ET1	EINT1	ET0	EINT0	00000000b
IE1	A9H	Interrupt Enable Register 1	-	-	-	ETK	-	EBTM	EPWM	ESSI	xxx0x000b
ADCCFG2	AAH	ADC Configuration Register 2	AINX[1:0]		-	LOWSP[2:0]			ADCCK[1:0]		00x00000b
ADCCFG0	ABH	ADC Configuration Register 0	EAINx[7:0]								00000000b
ADCCON	ADH	ADC Control Register	ADCEN	ADCS	ADCIF	ADCIS[4:0]					00000000b
ADCVL	AEH	ADC result Register	ADCV[3:0]				-	-	-	-	1111xxxxb
ADCVH	AFH	ADC result Register	ADCV[11:4]								11111111b
IP	B8H	Interrupt Priority Control Register	-	IPADC	IPT2	IPUART	IPT1	IPINT1	IPT0	IPINT0	x0000000b
IP1	B9H	Interrupt Priority Control Register 1	-	-	-	IPTK	-	IPBTM	IPPWM	IPSSI	xxx0x000b
INT0F	BAH	INT0 Falling-Edge Interrupt Control Register	INT0F7	INT0F6	INT0F5	INT0F4	INT0F3	INT0F2	INT0F1	INT0F0	00000000b
INT0R	BBH	INT0 Rising-edge Interrupt Control Register	INT0R7	INT0R6	INT0R5	INT0R4	INT0R3	INT0R2	INT0R1	INT0R0	00000000b
INT1F	BCH	INT1 Falling-edge Interrupt Control Register	-	-	INT1F5	INT1F4	INT1F3	INT1F2	INT1F1	INT1F0	xx000000b

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Symbol	Address	Description	7	6	5	4	3	2	1	0	Power-On Initial Value
INT1R	BDH	INT1 Rising-edge Interrupt Control Register	-	-	INT1R5	INT1R4	INT1R3	INT1R2	INT1R1	INT1R0	xx000000b
T2CON	C8H	Timer 2 Control Register	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2	00000000b
T2MOD	C9H	Timer 2 Working Mode Register	TXFD	-	EPWM21	EPWM20	INV21	INV20	T2OE	DCEN	0x000000b
RCAP2L	CAH	Timer 2 Reload Lower 8 Bits	RCAP2L[7:0]								00000000b
RCAP2H	CBH	Timer 2 Reload High 8 Bits	RCAP2H[7:0]								00000000b
TL2	CCH	Timer 2 Lower 8 Bits	TL2[7:0]								00000000b
TH2	CDH	Timer 2 High 8 Bits	TH2[7:0]								00000000b
BTMCON	CEH	Low-Frequency Timer Control Register	ENBTM	BTMIF	-	-	BTMFS[3:0]				00xx0000b
WDTCON	CFH	WDT Control Register	-	-	-	CLRWDT	-	WDTCKS[2:0]			xxx0x000b
PSW	D0H	Program Status Word Register	CY	AC	F0	RS1	RS0	OV	F1	P	00000000b
PWMCFG	D1H	PWM Setting Register	INV7	INV6	INV5	INV4	INV3	INV2	INV1	INV0	00000000b
PWMCON0	D2H	PWM Control Register 0	ENPWM	PWMIF	PWMCK[1:0]		-	-	PWMMD[1:0]		0000xx00b
PWMCON1	D3H	PWM Control Register 1	ENPWM7	ENPWM6	ENPWM5	ENPWM4	ENPWM3	ENPWM2	ENPWM1	ENPWM0	00000000b
PWMPDL	D4H	PWM Period Register Lower 8 Bits	PWMPDL[7:0]								00000000b
PWMPDH	D5H	PWM Period Register High 8 Bits	PWMPDH[7:0]								00000000b
PWMDFR	D6H	PWM Dead Time Setting Register	PDF[3:0]				PDR[3:0]				00000000b
PWMFLT	D7H	PWM Fault Detection Configuration Register	FLTEN1	FLTSTA1	FLTMD1	FLTLV1	-	-	FLTDT1[1:0]		0000xx00b
P5	D8H	P5 Port Data Register	-	-	-	-	-	-	P51	P50	xxxxxx00b
P5CON	D9H	P5 Port Input/Output Control Register	-	-	-	-	-	-	P5C1	P5C0	xxxxxx00b
P5PH	DAH	P5 Port Pull-Up Resistor Control Register	-	-	-	-	-	-	P5H1	P5H0	xxxxxx00b
ACC	E0H	Accumulator	ACC[7:0]								00000000b
EXA0	E9H	Extended accumulator 0	EXA[7:0]								00000000b
EXA1	EAH	Extended accumulator 1	EXA[15:8]								00000000b
EXA2	EBH	Extended accumulator 2	EXA[23:16]								00000000b
EXA3	ECH	Extended accumulator 3	EXA[31:24]								00000000b
EXBL	EDH	Extended Register B L	EXB [7:0]								00000000b
EXBH	EEH	Extended Register B H	EXB [15:8]								00000000b
OPERCON	EFH	Operation Control Register	OPERS	MD	-	-	-	-	CRCRST	CRCSTA	00xxxx00b
B	F0H	Register B	B[7:0]								00000000b
IAPKEY	F1H	IAP Protection Register	IAPKEY[7:0]								00000000b
IAPADL	F2H	IAP Write Address Low Byte Register	IAPADR[7:0]								00000000b
IAPADH	F3H	IAP Write Address High Byte Register	-	-	IAPADR[13:8]						xx000000b
IAPADE	F4H	IAP Write Extended Address Register	IAPADER[7:0]								00000000b
IAPDAT	F5H	IAP Data Register	IAPDAT[7:0]								00000000b
IAPCTL	F6H	IAP Control Register	BTLD	ERASE	PERASE	SERASE	PRG	-	CMD[1:0]		00000x00b
EXADH	F7H	External SRAM Operation Address Most Significant Bit	-	-	-	-	-		EXADH [1:0]		xxxxxx00b
CRCINX	FCH	CRC Pointer	CRCINX[7:0]								00000000b
CRCREG	FDH	CRC Register	CRCREG[7:0]								nnnnnnnnb
OPINX	FEH	Option Pointer	OPINX[7:0]								00000000b
OPREG	FFH	Option Register	OPREG[7:0]								nnnnnnnnb

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6.2.1 42-byte Register Extended RAM

6.2.1.1 General LED display RAM (400H to 40FH) @ DMOD=0

Address	Register Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
400H	COM0	S7	S6	S5	S4	S3	S2	S1	S0
401H		-	-	-	-	S11	S10	S9	S8
402H	COM1	S7	S6	S5	S4	S3	S2	S1	S0
403H		-	-	-	-	S11	S10	S9	S8
404H	COM2	S7	S6	S5	S4	S3	S2	S1	S0
405H		-	-	-	-	S11	S10	S9	S8
406H	COM3	S7	S6	S5	S4	S3	S2	S1	S0
407H		-	-	-	-	S11	S10	S9	S8
408H	COM4	S7	S6	S5	S4	S3	S2	S1	S0
409H		-	-	-	-	S11	S10	S9	S8
40AH	COM5	S7	S6	S5	S4	S3	S2	S1	S0
40BH		-	-	-	-	S11	S10	S9	S8
40CH	COM6	S7	S6	S5	S4	S3	S2	S1	S0
40DH		-	-	-	-	S11	S10	S9	S8
40EH	COM7	S7	S6	S5	S4	S3	S2	S1	S0
40FH		-	-	-	-	S11	S10	S9	S8

6.2.1.2 Bidirectional drive mode LED display RAM (400H to 417H) @ DMOD=1

Note: Each byte from 408H to 40FH has all 8 bits valid.

Address	Register Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
400H	LED0-	7	6	5	4	3	2	1	-
401H		-	-	-	-	11	10	9	8
402H	LED1-	19	18	17	16	15	14	-	0
403H		-	-	-	-	23	22	21	20
404H	LED2-	31	30	29	28	27	-	13	12
405H		-	-	-	-	35	34	33	32
406H	LED3-	43	42	41	40	-	26	25	24
407H		-	-	-	-	47	46	45	44
408H	LED4-	55	54	53	-	39	38	37	36
409H		-	-	-	-	59	58	57	56
40AH	LED5-	67	66	-	52	51	50	49	48
40BH		-	-	-	-	71	70	69	68
40CH	LED6-	79	-	65	64	63	62	61	60
40DH		-	-	-	-	83	82	81	80
40EH	LED7-	-	78	77	76	75	74	73	72
40FH		-	-	-	-	95	94	93	92
410H	LED8-	91	90	89	88	87	86	85	84
411H		-	-	-	-	107	106	105	-
412H	LED9-	103	102	101	100	99	98	97	96
413H		-	-	-	-	119	118	-	104
414H	LED10-	115	114	113	112	111	110	109	108
415H		-	-	-	-	131	-	117	116
416H	LED11-	127	126	125	124	123	122	121	120
417H		-	-	-	-	-	130	129	128

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6.2.1.3 PWM0 Duty Cycle Adjustment Register (R/W)

Address	7	6	5	4	3	2	1	0	Power-On Initial Value
418H	PDT00[15:8]								00000000b
419H	PDT00[7:0]								00000000b
41AH	PDT01[15:8]								00000000b
41BH	PDT01[7:0]								00000000b
41CH	PDT02[15:8]								00000000b
41DH	PDT02[7:0]								00000000b
41EH	PDT03[15:8]								00000000b
41FH	PDT03[7:0]								00000000b
408H	PDT07[15:8]								00000000b
409H	PDT07[7:0]								00000000b
40AH	PDT06[15:8]								00000000b
40BH	PDT06[7:0]								00000000b
40CH	PDT05[15:8]								00000000b
40DH	PDT05[7:0]								00000000b
40EH	PDT04[15:8]								00000000b
40FH	PDT04[7:0]								00000000b

6.2.1.4 PWM2 Duty Cycle Adjustment Register (R/W)

Address	7	6	5	4	3	2	1	0	Power-On Initial Value
420H	PDT20[15:8]								00000000b
421H	PDT20[7:0]								00000000b
422H	PDT21[15:8]								00000000b
423H	PDT21[7:0]								00000000b

6.2.1.5 PORT Mapped Register (R/W)

The SSICK0, SSITX0, SSIRX0, TXD0, RXD0, and PWM21 Ports of the SC92R425B support full Pin mapping. Users can set the mapped Port locations through the following registers.

Note: Only 5 bits are valid in each of the following six addresses:

Symbol	Address	Description	7	6	5	4	3	2	1	0	Power-On Initial Value
SPOS_PWM21	424H	PWM21 Mapping Register	-	-	-	PWM21SCL[4:0]					xxx00110b
SPOS_SSICK	425H	SSI CLK Mapping Register	-	-	-	SSICKSEL[4:0]					xxx00101b
SPOS_SSITX	426H	SSI TX Mapping Register	-	-	-	SSITXSEL[4:0]					xxx01000b
SPOS_SSIRX	427H	SSI RX Mapping Register	-	-	-	SSIRXSEL[4:0]					xxx01001b
SPOS_TX0	428H	UART0 TX Mapping Register	-	-	-	TX0SEL[4:0]					xxx10100b

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Symbol	Address	Description	7	6	5	4	3	2	1	0	Power-On Initial Value
SPOS_RX0	429H	UART0 RX Mapping Register	-	-	-	RX0SEL[4:0]					xxx10101b

Signal Mapping Settings

The signal functions corresponding to the signal mapping ports SSICK0, SSITX0, and SSIRX0 when SPI/TWI/UART is selected in the three-way Serial Port module are as follows:

- When SPI is selected: SSICK0 corresponds to SCK, SSITX0 corresponds to MOSI, and SSIRX0 corresponds to MISO.
- When TWI is selected: SSICK0 corresponds to SCL, and SSITX0 corresponds to SDA.
- When UART is selected: SSITX0 corresponds to TXD1, and SSIRX0 corresponds to RXD1.

To configure the mapping Pins, users can write values to the Mapping registers of the corresponding Ports. To map the PWM21 port to pin P0.1, first define a variable such as SPOS_PWM21 for the address of the PWM21 mapping register in RAM, then write the value 0x01 to SPOS_PWM21 to complete the mapping. The pin mappings and their corresponding setting values are shown in the table below, which also includes the default pin mappings for each port:

No.	Setting Value	Pin Mapping	Default Port-Communication	Default Port-PWM21
0	00000	P0.0	-	-
1	00001	P0.1	-	-
2	00010	P0.2	-	-
3	00011	P0.3	-	-
4	00100	P0.4	-	-
5	00101	P0.5	SSICK0	-
6	00110	P0.6	-	PWM21
7	00111	P0.7	-	-
8	01000	P2.0	SSITX0	-
9	01001	P2.1	SSIRX0	-
10	01010	P2.2	-	-
11	01011	P2.3	-	-
12	01100	P2.4	-	-
13	01101	P2.5	-	-
14	01110	P2.6	-	-
15	01111	P2.7	-	-
16	10000	P1.7	-	-
17	10001	P1.6	-	-
18	10010	P1.5	-	-
19	10011	P1.4	-	-
20	10100	P1.3	TXD0	-
21	10101	P1.2	RXD0	-
22	10110	P1.1	-	-
23	10111	P5.0	-	-
24	11000	P5.1	-	-
25	11001	P1.0	-	-
X	Others	Reserved	-	-

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6.2.2 Introduction to Common Special Function Registers of the 8051 CPU Core

6.2.2.1 Program Counter (PC)

The Program Counter PC is not an SFR Register. PC is 16 bits and is used to control the instruction execution sequence. After the Microcontroller is powered on or Reset, the PC value is 0000H, that is, the Microcontroller program starts execution at Address 0000H.

6.2.2.2 Accumulator ACC (E0H)

Accumulator ACC is one of the most commonly used Registers in an 8051-core microcontroller. The instruction set uses A as its mnemonic. It is commonly used to store operands and results involved in arithmetic or logic operations.

6.2.2.3 Register B (F0H)

Register B must be used with Accumulator A for multiplication and Division Operations. The multiplication Instruction MUL A, B multiplies the 8-bit unsigned numbers in Accumulator A and Register B. The low-order Byte of the resulting 16-bit Product is placed in A, and the Most Significant Bit Byte is placed in B. The DIV A, B division instruction divides A by B, placing the integer quotient in A and the remainder in B. The B Register can also be used as a general-purpose temporary Register.

6.2.2.4 Stack pointer SP (81H)

The Stack pointer is an 8-bit dedicated Register that indicates the location of the top of the Stack in general-purpose RAM. After the Microcontroller is Reset, the initial value of SP is 07H, so the Stack grows upward starting at 08H. 08H-1FH are Working Register Groups 1-3.

6.2.2.5 PSW (D0H) Program Status Word Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	CY	AC	F0	RS1	RS0	OV	F1	P
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

<table>
<tr><th>Bit Number</th><th>Bit Symbol</th><th>Description</th></tr>
<tr><td>7</td><td>CY</td><td>Flag
1: Set when the Most Significant Bit produces a Carry in addition or a borrow in subtraction
0: Set when the Most Significant Bit produces no Carry in addition or no borrow in subtraction</td></tr>
<tr><td>6</td><td>AC</td><td>Auxiliary Carry Flag (facilitates adjustment during BCD addition and subtraction)
1: Set when a Carry occurs at bit 3 during addition or a borrow occurs at bit 3 during subtraction
0: No borrow or Carry</td></tr>
<tr><td>5</td><td>F0</td><td>User Flag</td></tr>
<tr><td>4 ~ 3</td><td>RS1, RS0</td><td>Working Register Group selection bits:
<table>
<tr><th>RS1</th><th>RS0</th><th>Currently selected Working Register Group 0~3</th></tr>
<tr><td>0</td><td>0</td><td>Group 0 (00H~07H)</td></tr>
<tr><td>0</td><td>1</td><td>Group 1 (08H~0FH)</td></tr>
<tr><td>1</td><td>0</td><td>Group 2 (10H~17H)</td></tr>
<tr><td>1</td><td>1</td><td>Group 3 (18H~1FH)</td></tr>
</table></td></tr>
<tr><td>2</td><td>OV</td><td>Overflow Flag</td></tr>
<tr><td>1</td><td>F1</td><td>F1 Flag
User-Defined Flag</td></tr>
<tr><td>0</td><td>P</td><td>Parity Flag. This flag indicates the parity of the number of 1 s in the</td></tr>
</table>

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Bit Number	Bit Symbol	Description
		accumulator ACC. 1: The number of 1 s in ACC is odd 0: The number of 1 s in ACC is even (including 0)

6.2.2.6 Data Pointer DPTR (82H, 83H)

The Data Pointer DPTR is a 16-bit dedicated register consisting of the lower 8 bits DPL (82H) and the high 8 bits DPH (83H). DPTR is the only register in a traditional 8051-core microcontroller that can be operated on directly as a 16-bit register; DPL and DPH can also be operated on separately as bytes.

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7 Power supply, reset, and clock

7.1 Power supply circuit

The SC92R425B Power Supply core includes BG, LDO, POR, LVR, and other circuits, enabling reliable operation over the 2.4 to 5.5 V range. In addition, the IC has built-in calibrated, precise 1.024 V/ 2.4 V/ 2.048 V voltages that can be used as the ADC internal Reference voltage. For specific configuration details, see 18 ADC.

7.2 Power-on reset process

After the SC92R425B powers on and before the client software runs, it goes through the following process:

- Reset phase
- information load stage
- Normal Operation Phase

7.2.1 Reset phase

This means that the SC92R425B remains in Reset until the voltage supplied to the SC92R425B exceeds a certain level, and only then does the internal clock become active. The reset phase duration depends on the external power supply rise time. The reset phase completes only after the supply voltage reaches the internal POR threshold.

7.2.2 information load stage

There is a warm-up counter inside the SC92R425B. During the Reset phase, this warm-up counter is held at 0 until the voltage exceeds the POR voltage and the internal RC oscillator starts oscillating; the warm-up counter then begins Counting. When the internal warm-up counter reaches a certain count, each specified number of HRC clocks, one byte of Data is Read from the IFB (including Code Option) in Flash ROM and stored in an internal system Register. The reset signal is released after the warm-up is complete.

7.2.3 Normal operation phase

After the information load stage is complete, the SC92R425B begins Reading instruction code from Flash and enters the Normal Operation Phase. At this time, the LVR voltage is the setting value written by the user to Code Option.

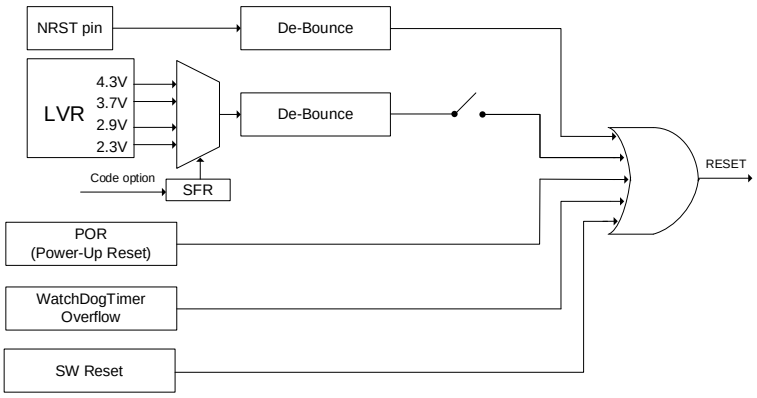
7.3 Reset modes

The SC92R425B has five reset modes. The first four are hardware resets:

1. External reset
2. Low voltage reset (LVR)
3. Power-on reset (POR)
4. Watchdog timer (WDT) reset
5. Software reset

The circuit structure of the SC92R425B reset section is shown below:

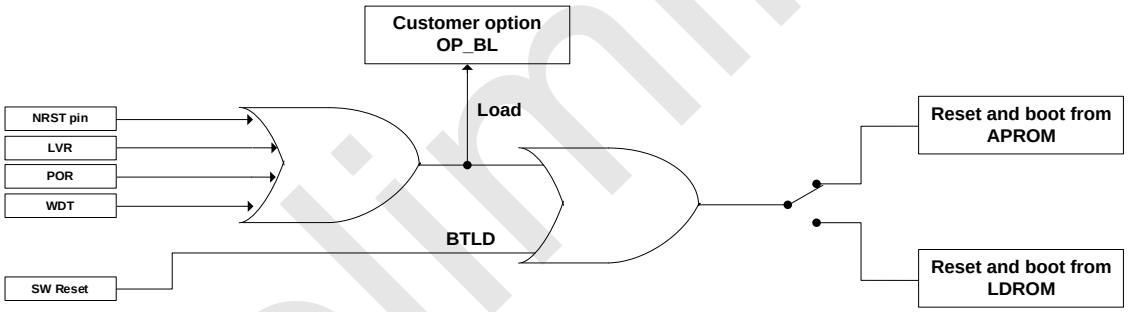
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SC92R425B reset circuit diagram

Boot Area After Reset:

1. After any of these four hardware resets-External reset (RST), Low voltage reset (LVR), Power-on reset (POR), or Watchdog (WDT)-the chip boots from the Boot Area (APROM/LDROM) configured by the user via OP_BL.
2. After a Software reset, the chip boots from the Boot Area (APROM/LDROM) configured by BTLD (IAPCTL.7).



SC92R425B boot area switching after reset

7.3.1 External reset

An External reset is performed by applying a reset pulse of a certain width to the SC92R425B via the external NRST pin.

Before programming the program, users can configure the Customer Option item in the Programming Host Software to use the P1.1 Pin as NRST (reset Pin).

7.3.2 Low voltage reset (LVR)

The SC92R425B has a built-in low-voltage reset circuit. There are four reset threshold voltage options: 4.3 V, 3.7 V, 2.9 V, and 2.3 V. The default is the Option value written by the user. When the VDD voltage falls below the low-voltage reset threshold for longer than T_{LVR}, a Reset is generated. Here, T_{LVR} is the LVR Debounce Time, approximately 30 μs.

OP_CTM0 (C1H@FFH) Customer Option Register 0 (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	ENWDT	ENXTL	SCLKS[1:0]		DISRST	DISLVR	LVRS[1:0]	
Read/Write	R/W	R/W	R/W		R/W	R/W	R/W	
Power-On	n	n	n		n	n	n	

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Bit Number	7	6	5	4	3	2	1	0
Initial Value								

Bit Number	Bit Symbol	Description
2	**DISLVR**	LVR Enable Setting 0: LVR enabled 1: LVR disabled
1 ~ 0	**LVRS [1:0]**	LVR Voltage Selection Control 11: 4.3 V Reset 10: 3.7 V Reset 01: 2.9 V Reset 00: 2.3 V Reset

7.3.3 Power-on reset (POR)

The SC92R425B has an internal power-on reset circuit. When the supply voltage VDD reaches the POR reset voltage, the system is automatically reset.

7.3.4 Watchdog reset WDT

The SC92R425B has a WDT with an internal 32 kHz oscillator as its Clock Source. The user can select whether to enable the Watchdog reset function through the Programmer's Code Option.

OP_CTM0 (C1H@FFH) Customer Option Register 0 (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	ENWDT	ENXTL	SCLKS[1:0]		DISRST	DISLVR	LVRS[1:0]	
Read/Write	R/W	R/W	R/W		R/W	R/W	R/W	
Power-On Initial Value	n	n	n		n	n	n	

Bit Number	Bit Symbol	Description
7	**ENWDT**	WDT enable (this bit is loaded by the system with the value set in the user's Code Option) 1: WDT starts working 0: WDT is disabled

WDTCON (CFH) Watchdog Control Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	-	-	-	CLRWDT	-	WDTCKS[2:0]		
Read/Write	-	-	-	R/W	-	R/W		
Power-On Initial Value	x	x	x	0	x	0	0	0

Bit Number	Bit Symbol	Description
4	**CLRWDT**	WDT clear bit (writing 1 is effective) 1: The WDT Counter starts Counting from 0 This bit is automatically cleared to 0 by the system Hardware
2 ~ 0	**WDTCKS [2:0]**	Watchdog Clock selection WDTCKS[2:0] / WDT Overflow time 000 / 500ms 001 / 250ms 010 / 125ms 011 / 62.5ms

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Bit Number	Bit Symbol	Description
		100 31.5ms 101 15.75ms 110 7.88ms 111 3.94ms
7 ~ 5, 3	-	Reserved

7.3.5 Software reset

PCON (87h) Power Management Control Register (W only, *not readable *)

Bit Number	7	6	5	4	3	2	1	0
Symbol	SMOD	-	LDLOCK	-	RST	-	STOP	IDL
Read/Write	W	-	W	-	W	-	W	W
Power-On Initial Value	0	x	0	x	n	x	0	0

Bit Number	Bit Symbol	Description
3	**RST**	Software Reset Control Bit: Write status: 0: Program runs normally 1: After this bit is written to 1, the CPU is reset immediately

7.3.6 Initial reset state

When the SC92R425B is in the reset state, most registers return to their initial states. The watchdog WDT is disabled. The initial value of the Program Counter PC is 0000h, and the initial value of the Stack pointer SP is 07h. "Warm reset" (such as WDT reset, LVR, software reset) does not affect SRAM; the SRAM value always remains as it was before reset. SRAM contents are lost when the Supply Voltage drops so low that RAM can no longer retain its contents.

For the power-on reset initial values of SFR Registers, see Section 6.2.1 Special-Function Unit.

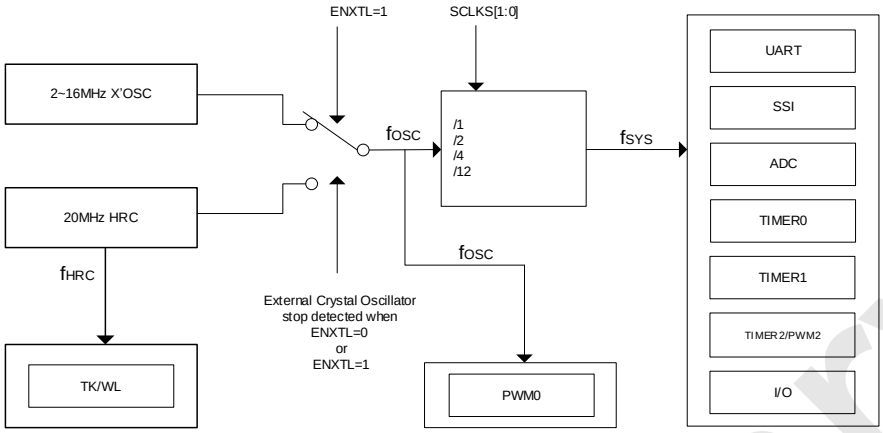
7.4 High-frequency system clock circuit

The SC92R425B integrates a high-precision HRC with an adjustable oscillation Frequency and a crystal oscillator circuit. The user can select either as the System Clock. The HRC is precisely calibrated at the factory to 20 MHz@5 V/25 ℃. The user can set the System Clock to 10/5/1.66 MHz through the Programmer's Code Option. Calibration filters out the effects of process variations on accuracy. The HRC drifts to some extent with changes in ambient temperature and Operating Voltage. Under typical conditions, voltage drift (2.4 V to 5.5 V) and temperature drift (-40 ℃ to 105 ℃) are generally within ±1%.

To enhance system reliability, the SC92R425B has a built-in System Clock Monitor Circuit. If the user selects the crystal oscillator as the System Clock Source and the crystal oscillator circuit stops oscillating, the System Clock Source will automatically switch to the built-in HRC and remain in this state until the next Reset.

Note: The Clock Source for the ADC and Touch circuit is fixed at f_{HRC} = 20 MHz and does not change when switching between the internal and external System Clock.

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SC92R425B internal clock relationships

OP_CTM0 (C1h@FFH) Customer Option Register 0 (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	ENWDT	ENXTL	SCLKS[1:0]		DISRST	DISLVR	LVRS[1:0]	
Read/Write	R/W	R/W	R/W		R/W	R/W	R/W	
Power-On Initial Value	n	n	n		n	n	n	

Bit Number	Bit Symbol	Description
6	ENXTL	External High-Frequency Crystal Oscillator Selection Switch 0: External High-Frequency Crystal Oscillator disabled; P5.0 and P5.1 are active 1: External High-Frequency Crystal Oscillator enabled; P5.0 and P5.1 are unavailable. **Note: The Clock Source for the ADC and Touch circuit is fixed at f_{HRC} = 20 MHz and does not change when switching between the internal and external System Clock.**
5 ~ 4	SCLKS[1:0]	System Clock Frequency selection: 00: System Clock Frequency is the High-frequency oscillator frequency divided by 1 01: System Clock Frequency is the High-frequency oscillator frequency divided by 2 10: System Clock Frequency is the High-frequency oscillator frequency divided by 4 11: System Clock Frequency is the High-frequency oscillator frequency divided by 12.

The SC92R425B has a special feature: users can adjust the HRC Frequency within a certain range by modifying the SFR value. Users can do this by configuring the OP_HRCR Register. For details on configuring this register, refer to section: 5.2.1 Option-related SFR Operation Description.

OP_HRCR (83H@FFH) System Clock Change Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	-	-	OP_HRCR[5:0]					
Read/Write	-	-	R/W					
Power-On Initial Value	x	x	n	n	n	n	n	n

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<table>
<tr><th>Bit Number</th><th>Bit Symbol</th><th>Description</th></tr>
<tr><td>5 ~ 0</td><td>OP_HRCR[5:0]</td><td>
HRC frequency adjustment register
Users can change the high-frequency oscillator frequency f_{HRC} by modifying the value of this Register, thereby changing the IC's System Clock Frequency f_{SYS}:
1. The initial power-on value OP_HRCR[s] of OP_HRCR[5:0] is fixed to ensure that f_{HRC} is 20 MHz; OP_HRCR[s] may vary from one IC to another
2. When the initial value is OP_HRCR[s], the IC's System Clock Frequency f_{SYS} can be set to an accurate 10/5/1.66 MHz using the Option item; each change of 1 in OP_HRCR [5:0] changes the f_{SYS}
The relationship between the OP_HRCR [5:0] value and the f_{SYS} output Frequency is as follows:
<table>
<tr><th>OP_HRCR [5:0] value</th><th>f_{SYS} Actual output frequency (10M as an example)</th></tr>
<tr><td>OP_HRCR [s]-n</td><td>10000*(1-0.5%*n)kHz</td></tr>
<tr><td>...</td><td>....</td></tr>
<tr><td>OP_HRCR [s]-2</td><td>10000*(1-0.5%*2) = 9900kHz</td></tr>
<tr><td>OP_HRCR [s]-1</td><td>10000*(1-0.5%*1) = 9950kHz</td></tr>
<tr><td>OP_HRCR [s]</td><td>10000kHz</td></tr>
<tr><td>OP_HRCR [s]+1</td><td>10000*(1+0.5%*1) = 10050kHz</td></tr>
<tr><td>OP_HRCR [s]+2</td><td>10000*(1+0.5%*2) = 10100kHz</td></tr>
<tr><td>...</td><td>...</td></tr>
<tr><td>OP_HRCR [s]+n</td><td>10000*(1+0.5%*n)kHz</td></tr>
</table>
Note:
1. After each Power-on, the value of OP_HRCR[5:0] is the value closest to 20 MHz for the High-frequency oscillator frequency f HRC
2. To ensure reliable IC operation, the IC's maximum operating frequency should preferably not exceed 110% of 10 MHz, i.e., 11 MHz
3. Please confirm that changing the HRC Frequency will not affect other functions.
</td></tr>
</table>

7.5 Low-frequency oscillator and low-frequency clock timer

The SC92R425B has a built-in 32 kHz RC oscillator circuit, which serves as the Clock Source for the Low-Frequency Clock Timer Base Timer and WDT. Starting the Base Timer or enabling the WDT starts the 32 kHz Low-frequency oscillator.

The Low-Frequency Clock Timer Base Timer can wake the CPU from STOP mode and generate interrupts.

BTMCON (CEH)Low-Frequency Timer Control Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	ENBTM	BTMIF	-	-	BTMFS[3:0]			
Read/Write	R/W	R/W	-	-	R/W			
Power-On Initial Value	0	0	x	x	0	0	0	0

Bit Number	Bit Symbol	Description
7	**ENBTM**	Low-Frequency Base Timer Start Control

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Bit Number	Bit Symbol	Description
		0: Base Timer not started 1: Base Timer started
6	**BTMIF**	Base Timer Interrupt Request Flag This Flag is automatically cleared by Hardware when the CPU accepts the Base Timer interrupt.
3 ~ 0	**BTMFS [3:0]**	Low-Frequency Clock Interrupt Frequency Selection 0000: Generate an interrupt every 15.625 ms 0001: Generate an interrupt every 31.25 ms 0010: Generate an interrupt every 62.5 ms 0011: Generate an interrupt every 125 ms 0100: Generate an interrupt every 0.25 seconds 0101: Generate an Interrupt every 0.5 seconds 0110: Generate an Interrupt every 1.0 second 0111: Generate an Interrupt every 2.0 seconds 1000: Generate an Interrupt every 4.0 seconds 1001: Generate an Interrupt every 8.0 s 1010: Generate an Interrupt every 16.0 s 1011: Generate an Interrupt every 32.0 s 1100 to 1111: Reserved
5 ~ 4	**-**	Reserved

7.6 Stop mode and idle mode

The SC92R425B provides a Special Function Register, PCON. Configuring bits 0 and 1 of this Register controls the MCU's Operating Mode.

Writing 1 to PCON.1 stops the internal High-Frequency System Clock, putting the MCU into STOP mode to save power. In STOP mode, the SC92R425B can be woken up by external interrupts INT0 to 1, the Low-Frequency Clock Interrupt, or a TK interrupt. It can also be woken from STOP mode by an External reset.

Writing 1 to PCON.0 stops program execution and puts the device into IDLE mode, while peripherals and clocks continue running. All CPU states are saved before entering IDLE mode. The device can be woken up by any interrupt.

PCON (87H) Power Management Control Register (W, *not readable *)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	SMOD	-	LDLOCK	-	RST	-	STOP	IDL
Read/Write	W	-	W	-	W	-	W	W
Power-On Initial Value	0	x	0	x	n	x	0	0

Bit Number	Bit Symbol	Description
1	**STOP**	STOP Mode Control 0: Normal operating mode 1: Energy-Saving Mode; the High-frequency oscillator stops running, while the Low-frequency oscillator and WDT can be enabled or disabled according to the settings.
0	**IDL**	IDLE Mode Control 0: Normal operating mode 1: Energy-Saving Mode; program execution stops, while peripherals and clocks continue running. All CPU states are saved before entering IDLE mode.

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Note: When configuring the MCU to enter STOP or IDLE mode, the instruction that sets the PCON register must be followed by 8 NOP instructions. No other instructions may immediately follow; otherwise, subsequent instructions may not execute correctly after wake-up!

For detailed examples, refer to the SC92 F_Lib file.

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8 Central processing unit CPU and instruction set

8.1 CPU

The CPU used in the SC92R425B is a high-speed 1T standard 8051 core, and its instruction set is fully compatible with that of traditional 8051-core microcontrollers.

8.2 Addressing modes

The addressing modes of the SC92R425B 1T 8051 CPU instructions are: ① Immediate Addressing ② Direct Addressing ③ Indirect Addressing ④ Register Addressing ⑤ Relative Addressing ⑥ Indexed Addressing ⑦ Bit Addressing

8.2.1 Immediate addressing

Immediate Addressing is also called immediate (number) addressing. The Operand used in the operation is specified directly in the Instruction, as in the following example:

MOV A, #50H (This Instruction transfers the immediate number 50H to Accumulator A)

8.2.2 Direct addressing

In Direct Addressing Mode, the Instruction Operand field specifies the Address of the Operand involved in the operation. Direct Addressing Mode can only be used to represent Special Function Registers, Internal Data Registers, and the Bit address space. Special Function Registers and the Bit address space can only be accessed using Direct Addressing Mode. Examples are as follows:

ANL 50H, #91H (The value in location 50H is ANDed with the immediate value 91H, and the result is stored in location 50H. Here, 50H is the direct Address, indicating a location in the Internal Data Register RAM.)

8.2.3 Indirect addressing

Indirect Addressing is indicated by placing the "@" symbol before R0 or R1. Assume the Data in R1 is 40H and the Data in internal Data memory location 40H is 55H; the Instruction is

MOV A, @R1 (transfer Data 55H to Accumulator A).

8.2.4 Register addressing

Register addressing operates on the contents of the selected working registers R7 to R0, Accumulator A, general-purpose Register B, Address Register, and Carry flag C. Registers R7 to R0 are specified by the lower 3 bits of the instruction code, while ACC, B, DPTR, and Carry flag C are implicit in the instruction code. Therefore, register addressing also includes an implicit addressing mode. The register bank is selected by RS1 and RS0 in the Program Status Word Register PSW. The registers specified by the instruction operands refer to registers in the current bank.

INC R0 means (R0)+1→R0

8.2.5 Relative addressing

Relative addressing adds the current value in the Program Counter (PC) to the number specified by the instruction's second byte, and uses the result as the branch address of the branch instruction. The branch address is also called the branch destination address; the current value in the PC is the base address, and the number specified by the instruction's second byte is the offset. Because the destination address is relative to the base address in the PC, this addressing mode is called relative addressing. The offset is a signed number, with a range of +127 to −128. This addressing mode is mainly used for branch instructions.

JC $+50H

This means that if the Carry flag C is 0, the contents of the Program Counter (PC) remain unchanged; that is, no branch occurs. If Carry flag C is 1, the destination address of this branch instruction is the result of adding 50H to the current value in PC and the Base address.

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8.2.6 Indexed addressing

In indexed addressing, the instruction operand specifies an index register that holds the indexed base address. In indexed addressing, the offset is added to the index base value, and the result is used as the operand address. The index registers are the Program Counter (PC) and the DPTR Address Register.

```
MOVC   A, @A+DPTR
```

This indicates that Accumulator A is the offset register. Its contents are added to the contents of the DPTR Address Register, and the result is used as the operand address. The value in that location is retrieved and loaded into Accumulator A.

8.2.7 Bit addressing

Bit Addressing refers to the addressing mode used to perform bit operations on internal data RAM and Special Function Registers that support bit operations. When performing bit operations, the Carry flag C serves as the bit-operation accumulator. The Instruction Operand specifies the bit address directly, and the bit is then operated on according to the nature of the opcode. The encoding of a bit address is exactly the same as that of a byte address in Direct Addressing; the two are distinguished mainly by the nature of the operation Instruction, so take particular care when using them.

```
MOV    C, 20H        (Move the value of the bit-operation register at address 20H into Carry flag C.)
```

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9 Interrupt

The SC92R425B microcontroller provides 11 interrupt sources: Timer0 to 2, INT0 to 1, ADC, PWM, UART, SSI, Base Timer, and TK/WL. These 11 interrupt sources are divided into two interrupt priority levels, and each can be individually set to High Priority or Low Priority. Each of the three external interrupts can be independently configured to trigger on a rising edge, falling edge, or dual-edge. Each interrupt has its own priority setting bit, Interrupt flag, Interrupt Vector, and Enable bit. The global interrupt enable bit EA can enable or disable all interrupts.

9.1 Interrupt source, vector

The Interrupt Sources, Interrupt Vectors, and related Control Bits of the SC92R425B are listed below:

Interrupt Source	Interrupt condition	Interrupt Flag	Interrupt Enable Control	Interrupt Priority Control	Interrupt Vector	Query Priority	Interrupt Number (C51)	Flag Clear Mode	Capability of Waking up STOP
INT0	External Interrupt 0 asserted	IE0	EINT0	IPINT0	0003H	1 (High)	0	H/W Auto	YES
Timer0	Timer0 Overflow	TF0	ET0	IPT0	000BH	2	1	H/W Auto	NO
INT1	External Interrupt 1 asserted	IE1	EINT1	IPINT1	0013H	3	2	H/W Auto	YES
Timer1	Timer1 Overflow	TF1	ET1	IPT1	001BH	4	3	H/W Auto	NO
UART	Receive or transmit complete	RI/TI	EUART	IPUART	0023H	5	4	Required user Clear	NO
Timer2	Timer2 Overflow	TF2	ET2	IPT2	002BH	6	5	Required user Clear	NO
ADC	ADC conversion complete	ADCIF	EADC	IPADC	0033H	7	6	Required user Clear	NO
SSI	Receive or transmit complete	SPIF/TWIF	ESSI	IPSSI	003BH	8	7	Required user Clear	NO
PWM0	PWM0 Overflow	PWMIF	EPWM	IPPWM	0043H	9	8	Required user Clear	NO
BTM	Base timer overflow	BTMIF	EBTM	IPBTM	004BH	10	9	H/W Auto	YES
TK/WL	Touch Key /Water Level Counter overflow	TKIF	ETK	IPTK	005BH	11	11	H/W Auto	YES

When EA=1 and each interrupt enable bit is set to 1, the interrupts occur as follows:

Timer interrupt: An interrupt is generated when Timer0 or Timer1 overflows, and interrupt flags TF0 and TF1 are set to "1". When the Microcontroller executes the Timer interrupt, interrupt flags TF0 and TF1 are automatically cleared to "0" by Hardware. An interrupt is generated when Timer2 overflows, and the interrupt flag TF2 is set to "1". After a Timer2 interrupt occurs, Hardware does not automatically clear the TF2 bit; this bit must be cleared by the user's software.

ADC interrupt: The ADC interrupt occurs when ADC Conversion is complete. Its interrupt flag is the ADC conversion complete flag ADCIF (ADCCON.5). When the user sets ADCS to start conversion, ADCIF is automatically set to "1" by hardware. After the ADC interrupt occurs, the user must clear it in software upon entering the Interrupt Service Routine.

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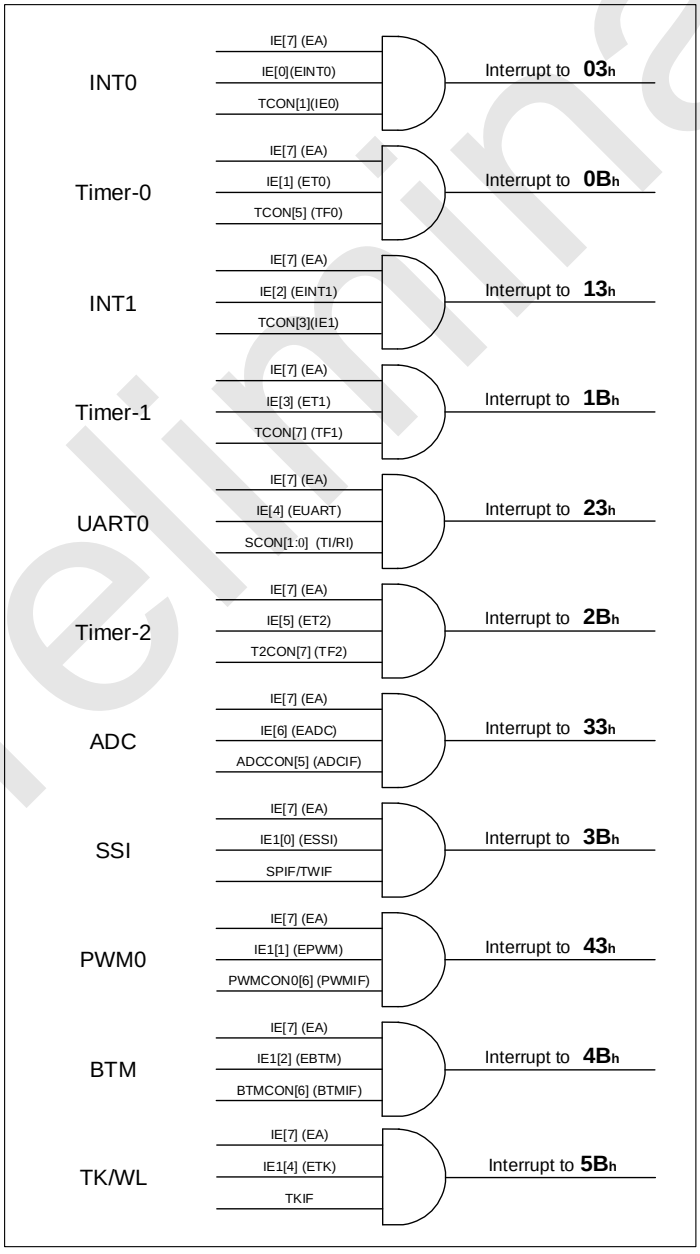
SSI interrupt: When one frame of data has been received or transmitted by SSI, the SPIF/TWIF bit is automatically set to "1" by hardware, generating an SSI interrupt. When the Microcontroller executes the SSI interrupt, the interrupt flag SPIF/TWIF must be cleared by the user's software.

PWM0 interrupt: When the PWM0 Counter overflows (that is, when the Counter counts past PWMPRD), the PWMIF bit (PWM Interrupt Flag) is automatically set to "1" by hardware, generating a PWM0 interrupt. After the PWM0 interrupt occurs, the user must clear it in software upon entering the Interrupt Service Routine.

External interrupts INT0 to 1: An external interrupt occurs when an interrupt condition is detected at an External interrupt input. INT0 has eight external interrupt sources, and INT1 has six. Users can configure rising-edge, falling-edge, or dual-edge interrupts as needed by setting the SFRs (INTxF and INTxR). Users can set the priority level of each interrupt using the IP Register. External interrupts INT0 to 1 can also wake up the Microcontroller from STOP mode.

9.2 Interrupt structure diagram

The SC92R425B interrupt structure is shown in the figure below:



SC92R425B interrupt structure and vectors

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9.3 Interrupt priority

The SC92R425B microcontroller has two interrupt priority levels. Interrupt requests from these sources can be programmed as high-priority or low-priority interrupts, enabling nesting of two levels of Interrupt Service Routines. A low-priority interrupt in progress can be interrupted by a high-priority interrupt request. However, it cannot be interrupted by another interrupt request of the same priority, and continues until completion. After executing the return instruction RETI and returning to the Main program, it can respond to a new interrupt request only after executing one more instruction.

In other words:

1. A low-priority interrupt can be interrupted by a high-priority interrupt request, but not vice versa
2. An interrupt in progress cannot be interrupted by an interrupt request of the same priority.

Interrupt Query Order: For same-priority interrupts occurring simultaneously on the SC92R425B microcontroller, the response priority follows the query priority order in the C51. Interrupts with lower query numbers are serviced first, while those with higher query numbers are serviced later.

9.4 Interrupt handling procedure

When an interrupt occurs and is acknowledged by the CPU, execution of the main program is interrupted, and the following operations are performed:

1. Complete the instruction currently being executed
2. Push the PC value onto the Stack to save the context
3. Load the Interrupt Vector address into the Program Counter (PC)
4. Execute the corresponding Interrupt Service Routine
5. End the Interrupt Service Routine and execute RETI
6. Pop the PC value from the Stack and return to the program that was executing before the interrupt.

During this process, interrupts of the same priority are not serviced immediately but are queued. Once the current interrupt handling completes, the system services pending interrupt requests.

9.5 Interrupt-related SFR registers

IE (A8H) Interrupt Enable Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	EA	EADC	ET2	EUART	ET1	EINT1	ET0	EINT0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7	**EA**	Global interrupt enable control 0: All interrupts disabled 1: All interrupts enabled
6	**EADC**	ADC interrupt enable control 0: ADC interrupt disabled 1: Enable an interrupt upon ADC conversion complete
5	**ET2**	Timer2 interrupt enable control 0: TIMER2 interrupt disabled 1: TIMER2 interrupt enabled
4	**EUART**	UART interrupt enable control 0: UART interrupt disabled 1: UART interrupt enabled

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Bit Number	Bit Symbol	Description
3	**ET1**	Timer1 interrupt enable control 0: TIMER1 interrupt disabled 1: TIMER1 interrupt enabled
2	**EINT1**	External interrupt 1 enable control 0: INT1 interrupt disabled 1: INT1 interrupt enabled
1	**ET0**	Timer0 interrupt enable control 0: TIMER0 interrupt disabled 1: TIMER0 interrupt enabled
0	**EINT0**	External interrupt 0 enable control 0: INT0 interrupt disabled 1: INT0 interrupt enabled

IP (B8H) Interrupt Priority Control Register (R/W)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	-	IPADC	IPT2	IPUART	IPT1	IPINT1	IPT0	IPINT0
Read/Write	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	x	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
6	**IPADC**	ADC interrupt priority selection 0: ADC interrupt priority is low 1: ADC interrupt priority is high
5	**IPT2**	Timer2 interrupt priority selection 0: Timer2 interrupt priority is low 1: Timer2 interrupt priority is high
4	**IPUART**	UART interrupt priority selection 0: UART interrupt priority is low 1: UART interrupt priority is high
3	**IPT1**	Timer1 interrupt priority selection 0: Timer1 interrupt priority is low 1: Timer1 interrupt priority is high
2	**IPINT1**	INT1 Counter interrupt priority selection 0: INT1 interrupt priority is low 1: INT1 interrupt priority is high
1	**IPT0**	Timer0 interrupt priority selection 0: Timer0 interrupt priority is low 1: Timer0 interrupt priority is high
0	**IPINT0**	INT0 Counter interrupt priority selection 0: INT0 interrupt priority is low 1: INT0 interrupt priority is high
7	**-**	Reserved

IE1 (A9H) Interrupt Control Register 1 (R/W)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	-	-	-	ETK	-	EBTM	EPWM	ESSI

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Bit Number	7	6	5	4	3	2	1	0
Read/Write	-	-	-	R/W	-	R/W	R/W	R/W
Power-On Initial Value	x	x	x	0	x	0	0	0

Bit Number	Bit Symbol	Description
4	**ETK**	Touch Key/Water Level interrupt enable control 0: Touch Key/Water Level interrupt disabled 1: Touch Key/Water Level interrupt enabled
2	**EBTM**	Base Timer interrupt Enable bit 0: Base Timer interrupt disabled 1: Base Timer interrupt enabled
1	**EPWM**	PWM interrupt Enable bit 0: PWM interrupt disabled 1: PWM interrupt enabled (reaches PWMPRD)
0	**ESSI**	SSI interrupt Enable bit 0: SSI interrupt disabled 1: SSI interrupt enabled
7 ~ 5, 3	**-**	Reserved

IP1 (B9H) Interrupt Priority Control Register 1 (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	-	-	-	IPTK	-	IPBTM	IPPWM	IPSSI
Read/Write	-	-	-	R/W	-	R/W	R/W	R/W
Power-On Initial Value	x	x	x	0	x	0	0	0

Bit Number	Bit Symbol	Description
4	**IPTK**	Touch Key/Water Level interrupt priority selection 0: Touch Key/Water Level interrupt priority is low 1: Touch Key/Water Level interrupt priority is high
2	**IPBTM**	Base Timer interrupt priority selection 0: Base Timer interrupt priority is low 1: Base Timer interrupt priority is high
1	**IPPWM**	PWM interrupt enable selection 0: PWM0 interrupt priority is low 1: PWM0 interrupt priority is high
0	**IPSSI**	Three-in-One Serial Port interrupt priority selection 0: SSI interrupt priority is low 1: SSI interrupt priority is high
7 ~ 5, 3	**-**	Reserved

TCON (88H) Timer Control Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	TF1	TR1	TF0	TR0	IE1	-	IE0	-
Read/Write	R/W	R/W	R/W	R/W	R/W	-	R/W	-
Power-On Initial Value	0	0	0	0	0	x	0	x

Bit Number	Bit Symbol	Description
3	**IE1**	INT1 request flag 0: No trigger event occurred 1: Selected trigger event occurred

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Bit Number	Bit Symbol	Description
		This bit is set by hardware when the selected edge event arrives on the external interrupt pin. Automatically cleared by hardware when the CPU services the interrupt.
1	**IE0**	INT0 request flag 0: No trigger event occurred 1: Selected trigger event occurred This bit is set by hardware when the selected edge event arrives on the external interrupt pin. Automatically cleared by hardware when the CPU services the interrupt.
2,0	**-**	Reserved

INT0F (BAH)INT0 falling-edge interrupt Control Register (R/W)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	INT0F7	INT0F6	INT0F5	INT0F4	INT0F3	INT0F2	INT0F1	INT0F0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7 ~ 0	**INT0Fn (n=0 to 7)**	INT0 falling-edge interrupt control 0: INT0n Falling-edge interrupt disabled 1: INT0n Falling-edge interrupt enabled

INT0R (BBH) INT0 Rising-edge Interrupt Control Register (R/W)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	INT0R7	INT0R6	INT0R5	INT0R4	INT0R3	INT0R2	INT0R1	INT0R0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7 ~ 0	**INT0Rn (n=0 to 7)**	INT0 Rising-edge interrupt control 0: INT0n Rising-edge interrupt disabled 1: INT0n Rising-edge interrupt enabled

INT1F (BCH) INT1 Falling-edge Interrupt Control Register (R/W)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	-	-	INT1F5	INT1F4	INT1F3	INT1F2	INT1F1	INT1F0
Read/Write	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	x	x	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
5 ~ 0	**INT1Fn (n=0 to 5)**	INT1 Falling-edge interrupt control 0: INT1n Falling-edge interrupt disabled 1: INT1n Falling-edge interrupt enabled
7 ~ 6	**-**	Reserved

INT1R (BDH) INT1 Rising-edge Interrupt Control Register (R/W)

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Bit Number	7	6	5	4	3	2	1	0
Symbol	-	-	INT1R5	INT1R4	INT1R3	INT1R2	INT1R1	INT1R0
Read/Write	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	x	x	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
5 ~ 0	**INT1Rn (n=0 to 5)**	INT1 Rising-edge interrupt control 0: INT1n Rising-edge interrupt disabled 1: INT1n Rising-edge interrupt enabled
7 ~ 6	**-**	Reserved

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10 Timer0,Timer1

The SC92R425B microcontroller has two internal 16-bit Timer/Counters, with Counting and Timing operating modes. A Control Bit, C/Tx, in the Special Function Register TMOD selects whether T0 and T1 operate as timers or counters. They are essentially add-up counters; only the source of the count differs. The timer source is the System Clock or its Divided Clock, whereas the counter source is Input Pulses from external pins. T0 and T1 start counting only when TRx=1.

In Counter Mode, each pulse on the P1.2/T0 and P1.3/T1 Pins increments the Count Values of T0 and T1 by 1, respectively.

In Timer mode, the TMCON Special Function Register selects whether the Counting Source for T0 and T1 is $f_{SYS}/12$ or f_{SYS} (f_{SYS} is the divided System Clock).

Timer/Counter T0 has 4 Operating Modes, and Timer/Counter T1 has 3 Operating Modes (mode 3 is unavailable):

1. Mode 0: 13-Bit Timer/Counter mode
2. Mode 1: 16-Bit Timer/Counter mode
3. Mode 2: 8-Bit Auto-Reload mode
4. Mode 3: Two 8-Bit Timer/Counter mode

In the above modes, Modes 0, 1, and 2 are the same for T0 and T1; Mode 3 is different.

10.1 T0 and T1 related special function registers

Symbol	Address	Description	7	6	5	4	3	2	1	0	Reset value
TCON	88H	Timer Control Register	TF1	TR1	TF0	TR0	IE1	-	IE0	-	00000x0xb
TMOD	89H	Timer Working Mode Register	-	C/T1	M11	M01	-	C/T0	M10	M00	x000x000b
TL0	8AH	Timer 0 Lower 8 Bits	TL0[7:0]								00000000b
TL1	8BH	Timer 1 Lower 8 Bits	TL1[7:0]								00000000b
TH0	8CH	Timer 0 High 8 Bits	TH0[7:0]								00000000b
TH1	8DH	Timer 1 High 8 Bits	TH1[7:0]								00000000b
TMCON	8EH	Timer Frequency Control Register	-	-	-	-	-	-	T1FD	T0FD	xxxxxx00b

The registers are described as follows:

TCON (88H) Timer Control Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	TF1	TR1	TF0	TR0	IE1	-	IE0	-
Read/Write	R/W	R/W	R/W	R/W	R/W	-	R/W	-
Power-On Initial Value	0	0	0	0	0	x	0	x

Bit Number	Bit Symbol	Description
7	**TF1**	T1 Overflow Interrupt Request Flag. When T1 overflows and an interrupt occurs, the hardware sets TF1 to "1" to request an interrupt; when the CPU responds, the hardware clears it to "0".
6	**TR1**	Timer1 Run Control Bit. This bit is set to 1 and cleared to 0 by

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Bit Number	Bit Symbol	Description
		software. When TR1=1, Timer1 starts counting. When TR1=0, Timer1 counting is disabled.
5	**TF0**	T0 Overflow Interrupt Request Flag. When Timer0 overflows, the hardware sets TF0 to “1” to request an interrupt. When the CPU acknowledges the interrupt, the hardware clears TF0 to "0".
4	**TR0**	Timer T0 Run Control Bit. This bit is set and cleared by software. When TR0=1, T0 is enabled to start counting. When TR0=0, T0 counting is disabled.
2,0	**-**	Reserved

TMOD (89H) Timer Working Mode Register (R/W)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	-	C/T1	M11	M01	-	C/T0	M10	M00
Read/Write	-	R/W	R/W	R/W	-	R/W	R/W	R/W
Power-On Initial Value	x	0	0	0	x	0	0	0
	T1				T0			

Bit Number	Bit Symbol	Description
6	**C/T1**	TMOD[6] controls Timer 1 0: Timer; the counting source for T1 is f_{SYS} Frequency division 1: Counter; the counting source for T1 is the external pin T1/P1.3
5 ~ 4	**M11, M01**	Timer/Counter 1 Mode Selection 00: 13-Bit Timer/Counter; the upper 3 bits of TL1 are invalid 01: 16-Bit Timer/Counter; TL1 and TH1 are fully valid 10: 8-Bit Auto-Reload Timer; on Overflow, the value stored in TH1 is automatically reloaded into TL1 11: Timer/Counter 1 disabled (counting stopped)
2	**C/T0**	TMOD[2] controls Timer 0 0: Timer; T0 counting source is f_{SYS} Frequency division 1: Counter; T0 counting source is external pin T0/P1.2
1 ~ 0	**M10, M00**	Timer/Counter 0 Mode Selection 00: 13-Bit Timer/Counter; upper 3 bits of TL0 are invalid 01: 16-Bit Timer/Counter; TL0 and TH0 are fully enabled 10: 8-bit Auto-Reload Timer; on overflow, the value stored in TH0 is automatically reloaded into TL0 11: Timer 0 operates as two 8-bit Timer/CountersTL0 operates as an 8-bit Timer/Counter, controlled by the control bits of standard Timer 0; TH0 is used only as an 8-bit timer, controlled by the Control Bit of Timer 1.
7, 3	**-**	Reserved

TMOD[0] to TMOD[2] in the TMOD Register set the Operating Mode of T0; TMOD[4] to TMOD[6] set the Operating Mode of T1.

The Timer and Counter functions of Tx are selected by the C/Tx Control Bit in the Special Function Register TMOD. M0x and M1x are used to select the Operating Mode of Tx. TRx controls T0 and T1 switching; T0 and T1 are enabled only when TRx=1.

TMCON (8EH) Timer Frequency Control Register (R/W)

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Bit Number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	T1FD	T0FD
Read/Write	-	-	-	-	-	-	R/W	R/W
Power-On Initial Value	x	x	x	x	x	x	0	0

Bit Number	Bit Symbol	Description
1	**T1FD**	T1 input Frequency selection Control 0: Timer1 frequency derived from f_{SYS}/12 1: Timer1 frequency derived from f_{SYS}
0	**T0FD**	Timer0 input frequency selection control 0: Timer0 frequency derived from f_{SYS}/12 1: Timer0 frequency derived from f_{SYS}
7 ~ 2	**-**	Reserved

IE (A8H) Interrupt Enable Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	EA	EADC	ET2	EUART	ET1	EINT1	ET0	EINT0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
3	**ET1**	Timer1 interrupt enable control 0: Disable TIMER1 interrupt 1: Enable TIMER1 interrupt
1	**ET0**	Timer0 interrupt Enable bit 0: Disable TIMER0 interrupt 1: Enable TIMER0 interrupt

IP (B8H) Interrupt Priority Control Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	-	IPADC	IPT2	IPUART	IPT1	IPINT1	IPT0	IPINT0
Read/Write	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	x	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
3	**IPT1**	Timer1 interrupt priority 0: Set Timer 1 interrupt priority to low 1: Set Timer 1 interrupt priority to high
1	**IPT0**	Timer0 interrupt priority 0: Set the Timer 0 interrupt priority to low 1: Set the Timer 0 interrupt priority to high

10.2 T0 operating mode

Timer/Counter 0 can operate in four different modes by setting M10 and M00 (TMOD[1] and TMOD[0]) in the TMOD Register.

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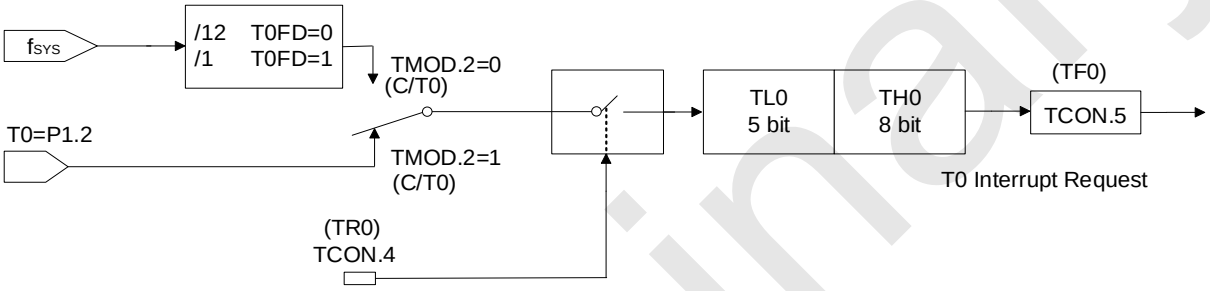
10.2.1 Operating mode 0: 13-Bit Counter/Timer

The TH0 Register stores the High 8 Bits of the 13-Bit Counter/Timer (TH0.7 to TH0.0), and TL0 stores the Lower 5 bits (TL0.4 to TL0.0). The upper three bits of TL0 (TL0.7 to TL0.5) are undefined and should be ignored when read. When the 13-Bit Timer/Counter increments and overflows, the system sets the Timer Overflow Flag TF0 to 1. If the Timer 0 interrupt is enabled, an interrupt is generated.

The C/T0 bit selects the clock input source for the Counter/Timer. If C/T0=1, a falling edge on the Timer T0 input pin T0 (P1.2) increments the Timer T0 Data Register by 1. If C/T0=0, the frequency-divided System Clock is selected as the Clock Source for Timer T0.

Setting TR0 to 1 starts Timer T0. Setting TR0 to 1 does not forcibly reset the timer, meaning that if TR0 is set to 1, the Timer Register will continue counting from its value when TR0 is last cleared. Therefore, the initial value of the Timer Register should be set before enabling the timer.

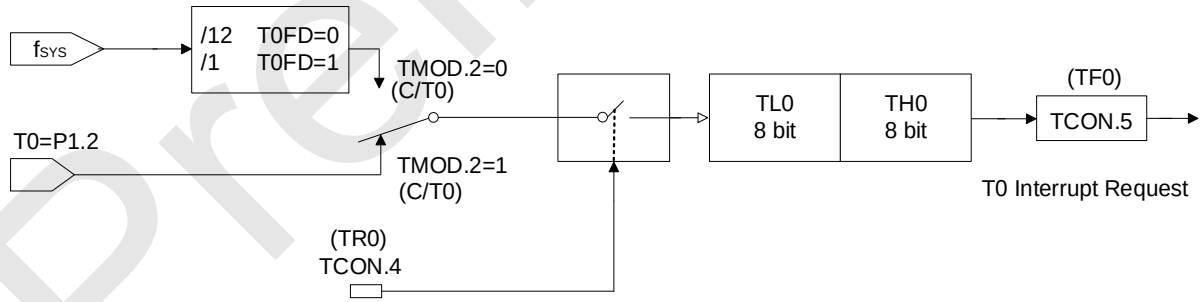
When used as a timer, T0FD can be configured to select the Frequency division ratio of the Clock Source.



Timer/Counter working mode 0: 13-bit Timer/Counter

10.2.2 Working mode 1: 16-Bit Counter/Timer

Modes 1 and 0 operate in the same way, except that Mode 1 uses a 16-bit (all 8 bits of TL0 are valid) Counter/Timer. The Counter/Timer is enabled and configured in the same way in both modes.



Timer/Counter working mode 1: 16-bit Timer/Counter

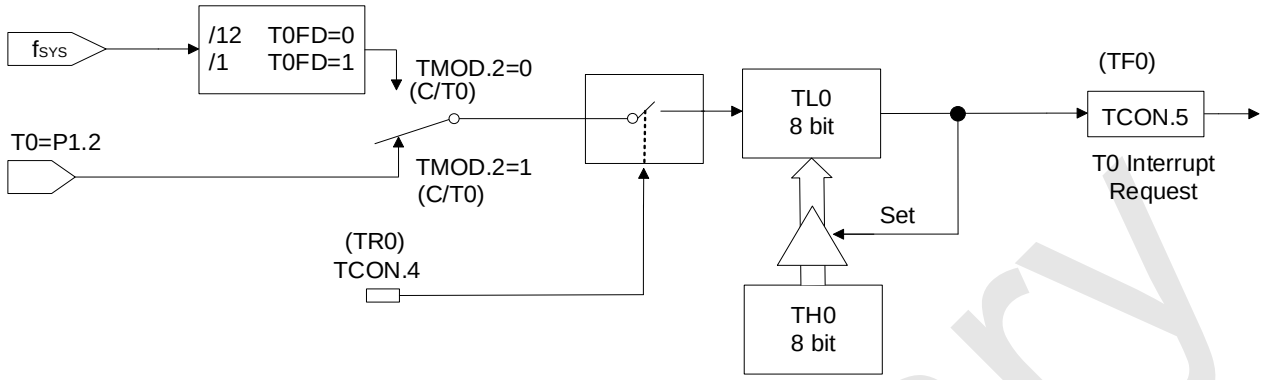
10.2.3 Working mode 2: 8-Bit Auto-Reload Counter/Timer

In Working Mode 2, Timer 0 is an 8-bit Auto-Reload Counter/Timer. TL0 stores the Count Value, and TH0 stores the Reload Value. When the counter in TL0 overflows to 0x00, the Timer Overflow Flag TF0 is set to 1, and the value in Register TH0 is reloaded into Register TL0. If the Timer interrupt is enabled, an interrupt will be generated when TF0 is set. The reload value in TH0 remains unchanged. TL0 must be initialized to the required value before the Timer is allowed to begin counting correctly.

Except for the Auto-Reload Function, the Timer/Counter in Operating Mode 2 is enabled and configured in the same way as in Modes 0 and 1.

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When used as a Timer, the ratio by which the System Clock f_{SYS} is divided to provide the Timer clock source can be selected by configuring register TMCON.0 (T0FD).



Timer/Counter operating mode 2: 8-bit Auto-Reload Timer/Counter

10.2.4 Operating mode 3: Two 8-Bit Counters/Timers (Timer 0 only)

In Operating Mode 3, Timer 0 is used as two independent 8-bit Counter/Timers, controlled separately by TL0 and TH0. TL0 is controlled by Timer 0's Control Bits (in TCON) and status bits (in TMOD): TR0, C/T0, and TF0. Timer 0 can be configured as either a Timer mode or Counter Mode using TMOD.2 (C/T0) for T0.

TH0 uses Timer 1's TCON control to configure the related controls, but TH0 is restricted to Timer mode and cannot be configured as Counter Mode using TMOD.2 (C/T0). TH0 is enabled by the Timer Control Bit TR1; TR1 must be set to 1. When an overflow occurs, TF1 is set, triggering an interrupt. The corresponding interrupt service for Timer1 is then executed.

When T0 is set to Operating Mode 3, the TH0 Timer uses T1's Interrupt resources and the Register in TCON. The T1 16-Bit Counter stops counting, which is equivalent to "TR1=0". When using the TH0 Timer, set TR1=1.

10.3 T1 operating mode

By setting M11 and M01 (TMOD[5] and TMOD[4]) in the TMOD Register, Timer/Counter 1 can implement three different Operating Modes.

10.3.1 Operating mode 0: 13-Bit Counter/Timer

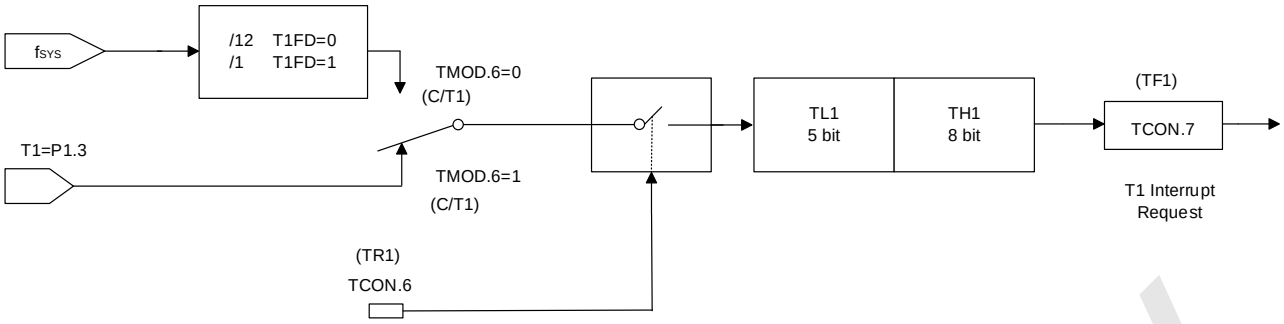
The TH1 Register stores the High 8 Bits of the 13-Bit Counter/Timer (TH1.7 to TH1.0); TL1 stores the Lower 5 bits (TL1.4 to TL1.0). The upper three bits of TL1 (TL1.7 to TL1.5) are undefined and should be ignored when read. When the 13-bit Timer/Counter overflows as it increments, the system sets the Timer Overflow Flag TF1 to 1. If the Timer 1 interrupt is enabled, an interrupt is generated. The C/T1 bit selects the Clock Source for the Counter/Timer.

If C/T1=1, a falling edge on the Timer 1 input pin T1 (P1.3) increments the Timer 1 Data Register by 1. If C/T1=0, a frequency-divided System Clock is selected as the Clock Source for Timer 1.

Setting TR1 to 1 starts the Timer. Setting TR1 to 1 does not forcibly reset the Timer, which means that if TR1 is set to 1, the Timer Register continues Counting from the value it had when TR1 was last cleared to 0. Therefore, the initial value of the Timer Register should be set before enabling the timer.

When used as a timer, T1FD can be configured to select the frequency division ratio of the clock source.

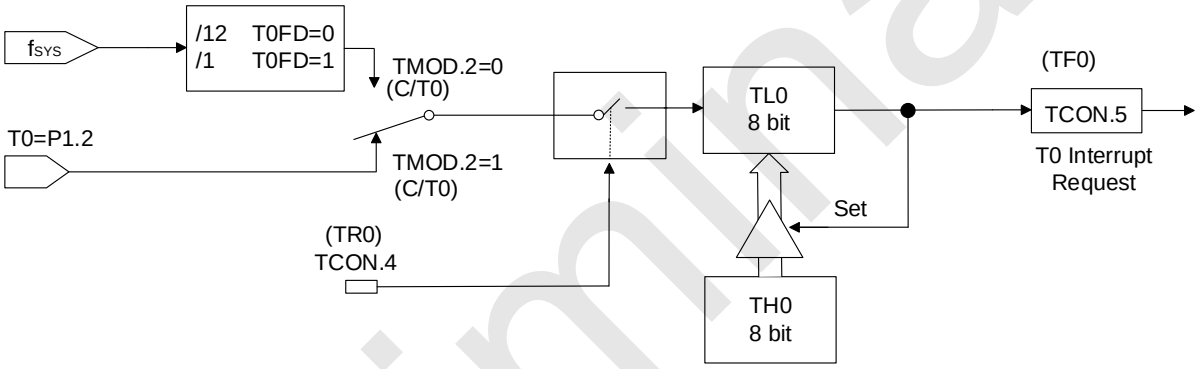
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Timer/Counter working mode 0: 13-bit Timer/Counter

10.3.2 Working mode 1: 16-Bit Counter/Timer

Except for using the 16-bit counter/timer mode (where all 8 bits of TL1 data are valid), modes 1 and 0 operate similarly. The methods to enable and configure the counter/timer are also the same.



Timer/Counter working mode 1: 16-bit Timer/Counter

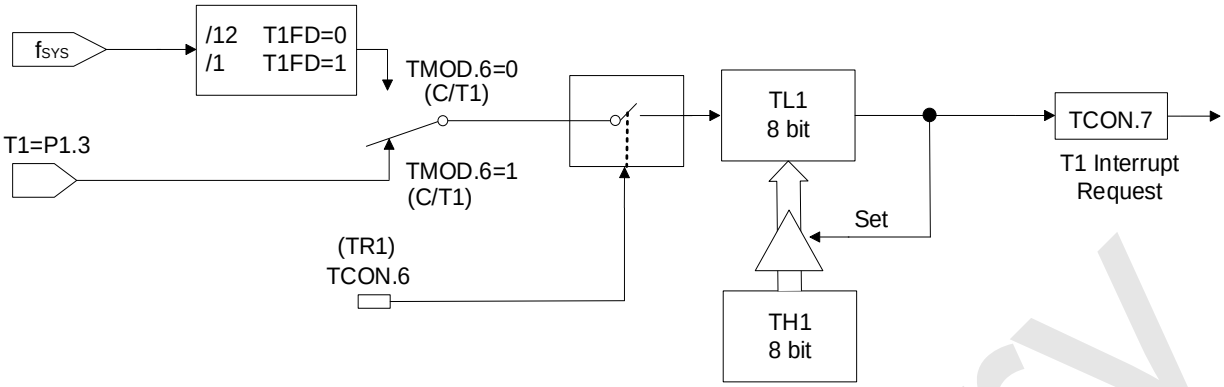
10.3.3 Operating mode 2: 8-Bit Auto-Reload Counter/Timer

In Operating Mode 2, Timer 1 is an 8-bit auto-reload counter/timer. TL1 stores the count value, and TH1 stores the reload value. When the count in TL1 overflows to 0x00, the Timer Overflow Flag TF1 is set to 1, and the value in register TH1 is reloaded into register TL1. If the timer interrupt is enabled, an interrupt will be generated when TF1 is set to 1, but the reload value in TH1 will not change. TL1 must be initialized to the required value before the timer is allowed to start counting correctly.

Except for the Auto-Reload Function, enabling and configuring the Counter/Timer in Operating Mode 2 is the same as in Modes 0 and 1.

When used as a timer, TMCON.1 (T1FD) can be configured to select the timer clock source as a divided portion of the system clock f_{SYS}.

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Timer/Counter operating mode 2: 8-bit Auto-Reload Timer/Counter

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11 Timer2

Timer2 in the SC92R425B microcontroller has two operating modes: Counting Method and Timing Mode. The Special Function Register T2CON contains a Control Bit, C/T2, to select whether T2 operates as a timer or a counter. They are essentially add-up counters; only the source of the count differs. The timer source is the System Clock or its Divided Clock, whereas the counter source is Input Pulses from external pins. TR2 controls whether T2 counts in Timer/Counter mode; T2 counts only when TR2=1.

In Counter Mode, the T2 count value increases by 1 for each pulse on the T2 pin.

In Timer mode, the TMCON Special Function Register can be used to select $f_{SYS}/12$ or f_{SYS}

Timer/Counter T2 has four Operating Modes:

1. Mode 0: 16-bit Capture mode
2. Mode 1: 16-bit Auto-Reload Timer mode
3. Mode 2: Baud rate generator mode
4. Mode 3: Programmable Clock Output mode

11.1 T2-related special function registers

Symbol	Address	Description	7	6	5	4	3	2	1	0	Reset value
T2CON	C8H	Timer 2 Control Register	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2	00000000b
T2MOD	C9H	Timer 2 Working Mode Register	TXFD	-	EPWM21	EPWM20	INV21	INV20	T2OE	DCEN	0x000000b
RCAP2L	CAH	Timer 2 Reload/Capture Lower 8 Bits	RCAP2L[7:0]								00000000b
RCAP2H	CBH	Timer 2 Reload/Capture High 8 Bits	RCAP2H[7:0]								00000000b
TL2	CCH	Timer 2 Lower 8 Bits	TL2[7:0]								00000000b
TH2	CDH	Timer 2 High 8 Bits	TH2[7:0]								00000000b
TMCON	8EH	Timer Frequency Control Register	-	-	-	-	-	-	T1FD	T0FD	xxxxxx00b

The registers are described as follows:

T2CON (C8H) Timer 2 Control Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7	**TF2**	Timer 2 Overflow Flag 0: No overflow (must be cleared to 0 by software) 1: Overflow (set to 1 by Hardware if RCLK = 0 and TCLK = 0)
6	**EXF2**	Flag indicating that an external event input on the T2EX pin (Falling edge) has been detected 0: No External Event Input (must be cleared to 0 by software) 1: External Input detected (set to 1 by Hardware if EXEN2 = 1)
5	**RCLK**	UART Receive Clock Control Bit

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Bit Number	Bit Symbol	Description
		0: Timer 1 generates the Receive baud rate 1: Timer 2 generates the Receive baud rate
4	**TCLK**	UART Transmit Clock Control Bit 0: Timer 1 generates the Transmit baud rate 1: Timer 2 generates the Transmit baud rate
3	**EXEN2**	External Event Input on the T2EX pin (Falling edge) as the Reload/Capture trigger enable/disable control: 0: Ignore events on the T2EX pin 1: When Timer 2 is not used as the UART Clock, a Falling edge detected on the T2EX pin generates a Capture or Reload
2	**TR2**	Timer 2 Start/Stop Control Bit 0: Stop Timer 2 1: Start Timer 2
1	**C/T2**	Timer 2 Timer/Counter Mode Select Bit 2 0: Timer mode; T2 pin used as an I/O port 1: Counter mode
0	**CP/RL2**	Capture/Reload mode select bit 0: 16-bit Timer/Counter with Reload function 1: 16-bit Timer/Counter with Capture function; T2EX is the Timer 2 External Capture Signal Input

T2MOD (C9H) Timer 2 working mode register (R/W)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	TXFD	-	EPWM21	EPWM20	INV21	INV20	T2OE	DCEN
Read/Write	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	x	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7	**TXFD**	T2 input frequency selection control 0: T2 Frequency sourced from f_{SYS}/12 1: T2 Frequency sourced from f_{SYS}
1	**T2OE**	Timer 2 output enable bit 0: Set T2 as a Clock input or I/O port 1: Set T2 as a Clock output
0	**DCEN**	Decrement Counting Enabled bit 0: Timer 2 operates as an increment counter 1: Timer 2 operates as an increment/decrement counter
6	**-**	Reserved

IE (A8H) Interrupt Enable Register (R/W)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	EA	EADC	ET2	EUART	ET1	EINT1	ET0	EINT0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

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Bit Number	Bit Symbol	Description
5	**ET2**	Timer2 interrupt enable control 0: Disable TIMER2 interrupt 1: Enable TIMER2 interrupt

IP (B8H) Interrupt Priority Control Register (R/W)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	-	IPADC	IPT2	IPUART	IPT1	IPINT1	IPT0	IPINT0
Read/Write	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	x	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
5	**IPT2**	Timer2 interrupt priority 0: Set the Timer 2 interrupt priority to low 1: Set the Timer 2 interrupt priority to high

11.2 T2 operating mode

The operating modes and configuration options for Timer 2 are shown in the table below:

C/$\overline{T2}$	**T2OE**	**DCEN**	**TR2**	**CP/$\overline{RL2}$**	**RCLK**	**TCLK**	**Mode**	
X	0	X	1	1	0	0	0	16-bit Capture
X	0	0	1	0	0	0	1	16-Bit Auto-Reload Timer
X	0	1	1	0	0	0		
X	0	X	1	X	1	X	2	Baud rate generator
					X	1		
0	1	X	1	X	0	0	3	For programmable clock use
					1	X	3	Programmable clock output with baud rate generator
					X	1		
X	X	X	0	X	X	X	X	Timer 2 stopped; T2EX path remains enabled
1	1	X	1	X	X	X		Not recommended for use

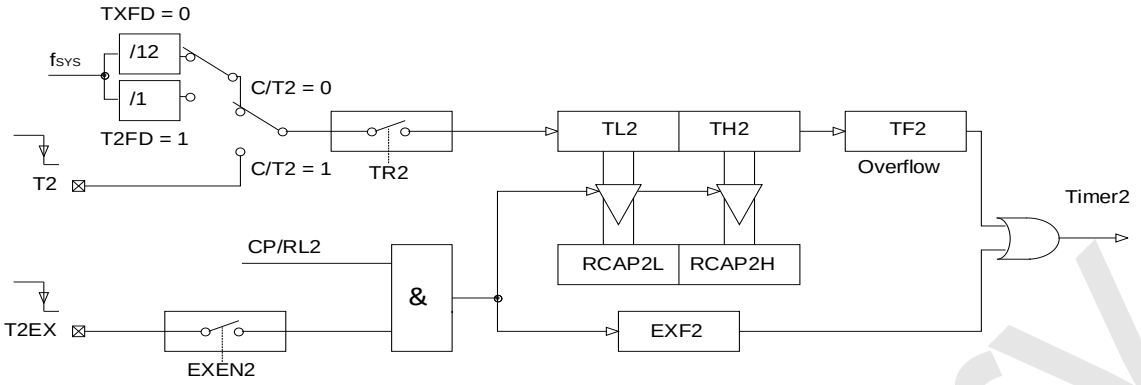
11.2.1 Operating mode 0: 16-bit Capture

In Capture mode, the EXEN2 bit in T2CON has two options.

If EXEN2 = 0, Timer 2 operates as a 16-bit timer or counter. If ET2 is enabled, Timer 2 can set TF2 on overflow to generate an interrupt.

If EXEN2 = 1, Timer 2 performs the same operation, but a Falling edge on the External Input T2EX can also cause the current values in TH2 and TL2 to be captured in RCAP2H and RCAP2L, respectively. In addition, a Falling edge on T2EX can set EXF2 in T2CON. If ET2 is enabled, the EXF2 bit also generates an interrupt, just like TF2.

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Mode 0: 16-bit Capture

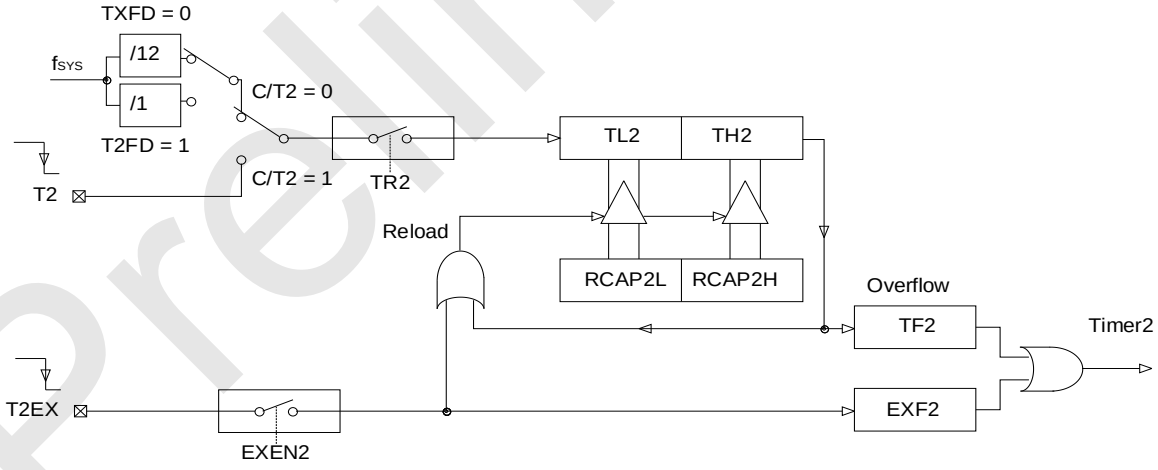
11.2.2 Operating mode 1: 16-Bit Auto-Reload Timer

In 16-bit Auto-Reload Mode, Timer 2 can be selected for Increment Counting or Decrement Count. This function is selected using the DCEN bit (Decrement Counting Enabled) in T2MOD. After a system Reset, the DCEN bit resets to 0, and Timer 2 defaults to Increment Counting. When DCEN is set to 1, whether Timer 2 increments or decrements depends on the level on the T2EX pin.

When DCEN = 0, select between the two options using the EXEN2 bit in T2CON.

If EXEN2 = 0, Timer 2 counts up to 0xFFFFH. Upon overflow, the TF2 bit is set, and the 16-bit value written by user software to the RCAP2H and RCAP2L registers is automatically loaded into the TH2 and TL2 registers.

If EXEN2 = 1, overflow or a falling edge on the T2EX pin can trigger a 16-bit reload. When a falling edge occurs on T2EX, the EXF2 bit is set. If ET2 is enabled, both the TF2 and EXF2 bits can generate an interrupt.



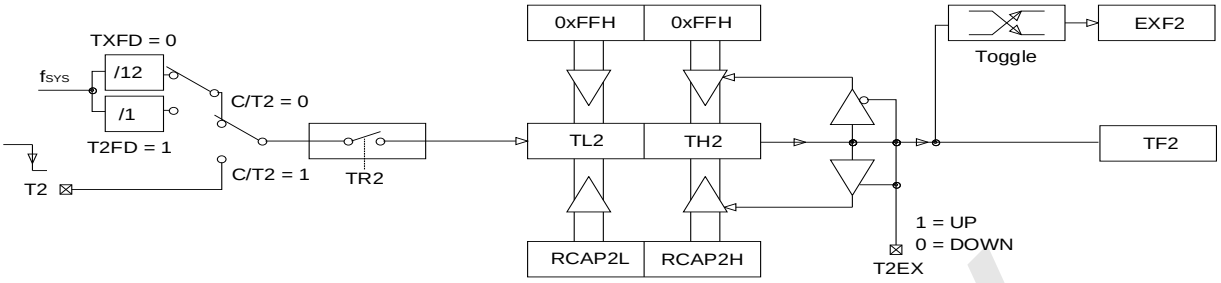
Mode 1: 16-bit Auto-Reload, DCEN = 0

Setting the DCEN bit allows Timer 2 to count up or down. When DCEN = 1, the T2EX pin controls the counting direction, and EXEN2 has no effect.

Setting T2EX to 1 enables Timer 2 Increment Counting. The timer overflows at 0xFFFFH, then sets the TF2 bit. The overflow can also reload the 16-bit value in RCAP2H and RCAP2L into the Timer Registers.

Setting T2EX to 0 enables Timer 2 Decrement Count. The timer overflows when the values of TH2 and TL2 equal those of RCAP2H and RCAP2L. The TF2 bit is set, and 0xFFFFH is reloaded into the Timer Registers. Whether or not Timer 2 overflows, the EXF2 bit is used as the 17th bit of the result. In this operating mode, EXF2 is not used as an Interrupt flag.

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Mode 1: 16-bit Auto-Reload DCEN = 1

11.2.3 Operating mode 2: Baud rate generator

By setting TCLK and/or RCLK in the T2CON Register, Timer 2 is selected as the Baud rate generator. The receiver and transmitter can use different Baud rates. If Timer 2 is used for the receiver or transmitter, Timer 1 is correspondingly used as the Baud rate generator for the other.

Setting TCLK and/or RCLK in the T2CON Register puts Timer 2 into Baud rate generator mode, which is similar to Auto-Reload Mode.

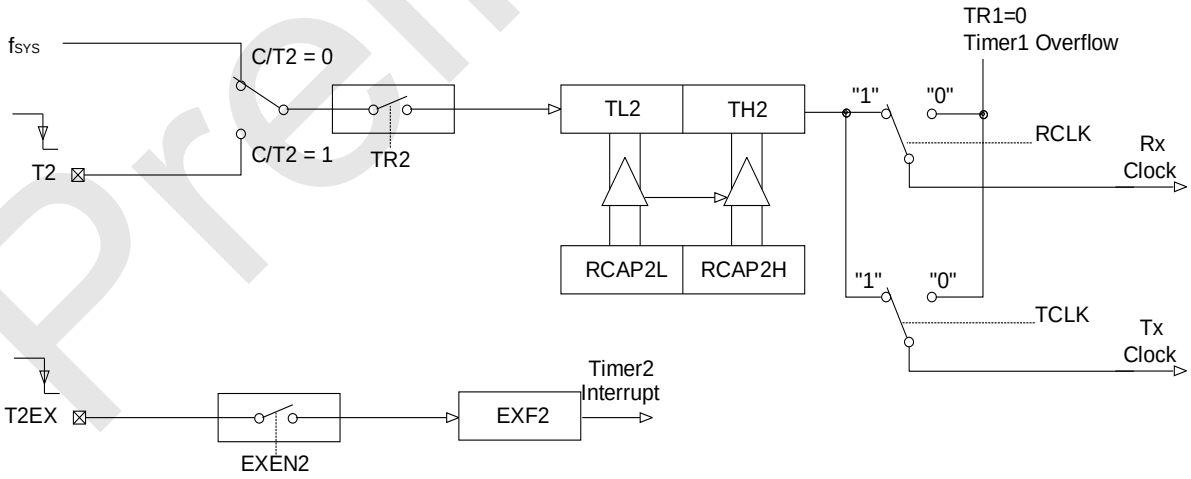
An overflow of Timer 2 reloads the values in the RCAP2H and RCAP2L Registers into the Timer 2 counter, but does not generate an interrupt.

If EXEN2 is set to 1, a falling edge on the T2EX pin sets EXF2, but does not trigger a reload. Therefore, when Timer 2 is used as a baud rate transmitter, T2EX can serve as an additional external interrupt

In UART modes 1 and 3, the baud rate is determined by the Timer 2 overflow rate according to the following equation:

$$\text{BaudRate} = \frac{f_{SYS}}{[\text{RCAP2H,RCAP2L}]}$$; (Note: [RCAP2H,RCAP2L] must be greater than 0x0010)

The schematic of Timer 2 operating as a baud rate generator is shown below:



Mode 2: Baud rate generator

11.2.4 Operating mode 3: Programmable Clock Output

In this mode, T2 can be programmed to output a clock with a 50% duty cycle: when C/ = 0; T2OE = 1, Timer 2 is enabled as a clock generator$\overline{T2}$

In this mode, T2 outputs a clock with a 50% duty cycle

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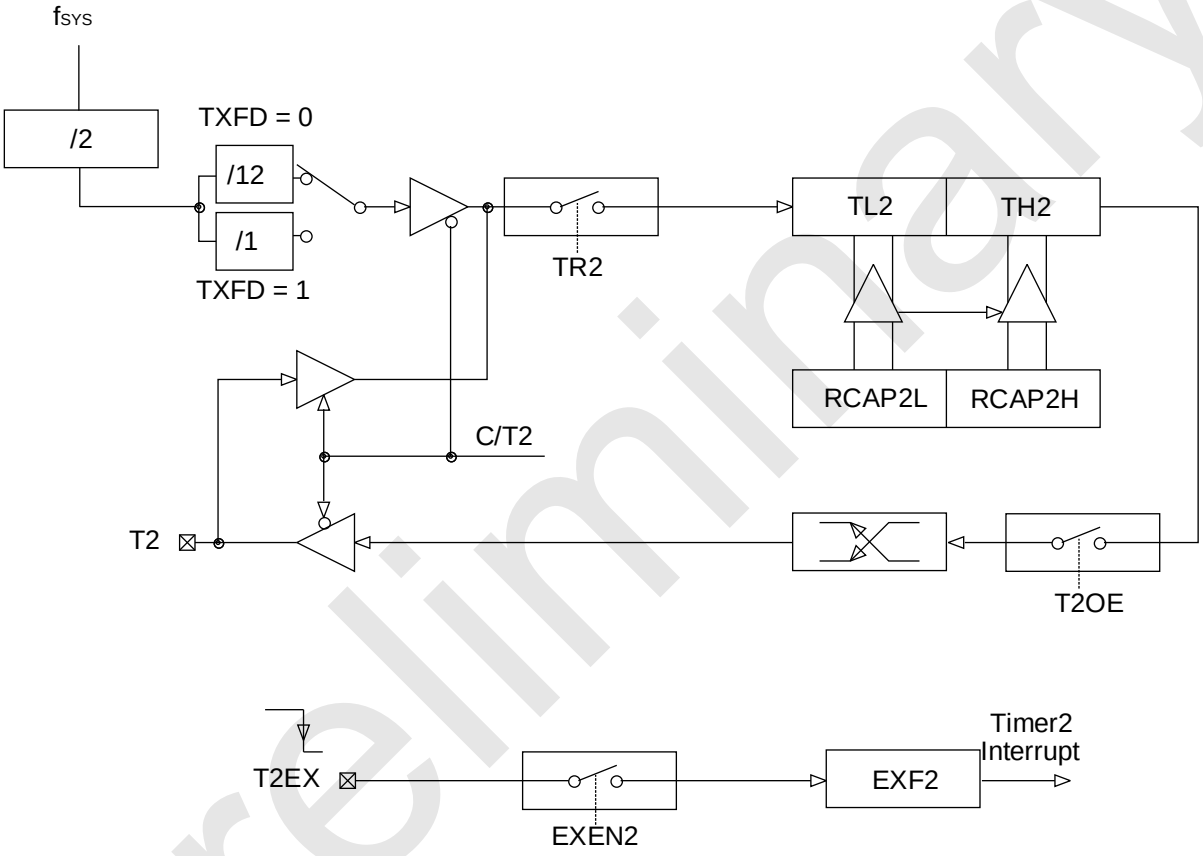
$$\text{Clock Out Frequency} = \frac{\text{fn2}}{(65536 - [\text{RCAP2H}, \text{RCAP2L}]) \times 4}$$

Where fn2 is the Timer 2 clock frequency:

$$\text{fn2} = \frac{f_{SYS}}{12};\text{TXFD} = 0$$

$$\text{fn2} = f_{SYS};\text{TXFD} = 1$$

Timer 2 overflow does not generate an interrupt; the T2 port serves as the clock output.



Mode 3: Programmable Clock Output

Note:

1. Both TF2 and EXF2 can generate a Timer 2 interrupt request, and they share the same vector address
2. TF2 and EXF2 can be set to 1 by software when an event occurs or at any other time; only software and Hardware Reset can clear them to 0
3. When EA = 1 and ET2 = 1, setting TF2 or EXF2 to 1 can trigger a Timer 2 Interrupt
4. When Timer 2 is used as a Baud rate generator, writing to TH2/TL2 or RCAP2H/RCAP2L affects baud rate accuracy and can cause Communication errors.

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12 Multiplier/Divider

The SC92R425B provides one 16-bit multiplier/divider consisting of extended accumulators EXA0 to EXA3, Extended Register B EXB, and the Operation Control Register OPERCON. Its hardware multiplier/divider does not use CPU cycles; the operation is performed in hardware and runs tens of times faster than software implementations. It can replace software for 16-bit×16-bit multiplication and 32-bit/16-bit division operations.

Symbol	Address	Description	7	6	5	4	3	2	1	0	Reset value
EXA0	E9H	Extended accumulator 0	EXA [7:0]								00000000b
EXA1	EAH	Extended accumulator 1	EXA [15:8]								00000000b
EXA2	EBH	Extended accumulator 2	EXA [23:16]								00000000b
EXA3	ECH	Extended accumulator 3	EXA [31:24]								00000000b
EXBL	EDH	Extended Register B L	EXB [7:0]								00000000b
EXBH	EEH	Extended Register B H	EXB [15:8]								00000000b
OPERCON	EFH	Operation Control Register	OPERS	MD	-	-	-	-	CRCRST	CRCSTA	00xxxx00b

OPERCON (EFH) Operation Control Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	OPERS	MD	-	-	-	-	CRCRST	CRCSTA
Read/Write	R/W	R/W	-	-	-	-	R/W	R/W
Power-On Initial Value	0	0	x	x	x	x	0	0

Bit Number	Bit Symbol	Description
7	**OPERS**	Multiplier/divider operation start trigger control (Operater Start) Write "1" to this bit to start one multiplier/divider calculation. This bit serves only as the trigger signal for starting the calculation; when it is zero, the calculation is complete. Only writing 1 to this bit is effective.
6	**MD**	Multiplication/Division Selection 0: Multiplication operation; write the multiplicand and multiplier, and read the product as follows: Byte / Operand: Byte 3 | Byte 2 | Byte 1 | Byte 0 16-bit Multiplicand: - | - | EXA1 | EXA0 16-bit Multiplier: - | - | EXBH | EXBL 32-bit Product: EXA3 | EXA2 | EXA1 | EXA0 1: For the division operation, the dividend and divisor are written, and the quotient and remainder are read, as follows: Byte / Operand: Byte 3 | Byte 2 | Byte 1 | Byte 0 32-bit Dividend: EXA3 | EXA2 | EXA1 | EXA0 16-bit Divisor: - | - | EXBH | EXBL 32-bit Quotient: EXA3 | EXA2 | EXA1 | EXA0 16-bit Remainder: - | - | EXBH | EXBL

Note:

1. **While an operation is in progress, do not read from or write to the EXA and EXB Data Registers.**
2. **The multiplier/divider operation takes 16/f_{SYS}.**

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13 General-purpose pulse width modulation counter PWM2

The SC92R425B provides 10 PWM channels, divided into two categories:

1. Multifunction PWM: 8 channels per group, namely PWM0, with output ports PWM00 to 07
2. General-Purpose PWM: 2 channels per group, namely PWM2, with outputs PWM20 to PWM21.

Note: The PWM2 Cycle Register shares TL2 and TH2 with Timer2. Therefore, once PWM2 is in use, do not change the Timer/Counter Value of Timer2; otherwise, the PWM period output will be abnormal!

13.1 PWM2 registers

Symbol	Address	Description	7	6	5	4	3	2	1	0	Reset value
T2CON	C8H	Timer 2 Control Register	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2	00000000b
T2MOD	C9H	Timer 2 Working Mode Register	TXFD	-	EPWM21	EPWM20	INV21	INV20	T2OE	DCEN	0x000000b
RCAP2L	CAH	Timer 2 Reload/Capture Lower 8 Bits	RCAP2L[7:0]								00000000b
RCAP2H	CBH	Timer 2 Reload/Capture High 8 Bits	RCAP2H[7:0]								00000000b
TL2	CCH	Timer 2 Lower 8 Bits	TL2[7:0]								00000000b
TH2	CDH	Timer 2 High 8 Bits	TH2[7:0]								00000000b

The registers are described as follows:

T2CON (C8H) Timer n Control Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
2	**TR2**	Timer 2 Start/Stop Control Bit 0: Stop Timer2 and stop the PWM2 Counter 1: Start Timer2 and enable the PWM2 Counter

When EPWM20 or EPWM21 is set to 1, Timer2 can enter PWM mode. In this mode, T2 and T2EX are invalid, and PWM20 and PWM21 can output PWM waveforms.

T2MOD (C9H) Timer n Working Mode Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	TXFD	-	EPWM21	EPWM20	INV21	INV20	T2OE	DCEN
Read/Write	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	x	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
5	**ENPWMn1**	PWMn1 waveform output selection 0: PWM21 output is disabled 1: The I/O pin assigned to PWM21 serves as the PWM waveform output port

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Bit Number	Bit Symbol	Description
4	**ENPWMn0**	PWMn0 waveform output selection 0: PWM20 output is disabled 1: The I/O pin assigned to PWM20 serves as the PWM waveform output port
3	**INVn1**	PWMn1 waveform output Reverse control 1: PWM21 waveform output is reversed 0: PWM21 waveform output is not reversed
2	**INVn0**	PWMn0 waveform output Reverse control 1: PWM20 waveform output is reversed 0: PWM20 waveform output is not reversed

The TH2 and TL2 counters count upward from 0. When the Count Value matches the value of the Duty cycle setting PDTxy [15:0], the PWM output changes state. The TH2 and TL2 counters then continue counting upward to the Auto-Reload Value PWMPDX, then start counting again from 0 and generate a count overflow event, completing one PWM period. If the Timer interrupt is enabled, a Timer interrupt is generated at this time.

PWM period T output by the Timer PWM calculation formula is as follows:

$$T_{PWM} = \frac{PWMPDX[15:0] + 1}{f_{SYS}}$$

Duty cycle duty calculation formula:

$$duty = \frac{PDTxy\ [15:0]}{PWMPDX[15:0] + 1}$$

The PWM period is set using the following Registers:

RCAP2H (CBH) PWMn Cycle Register High 8 Bits (R/W)

Note: The PWM2 Cycle Register is shared with Timer2. Therefore, once the user uses the PWM2 resource, the Timer2 Timer/Counter Value can no longer be changed; otherwise, the PWM period output will be abnormal!

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	PWMPDH2[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

RCAP2L (CAH) PWMn Cycle Register Lower 8 Bits (R/W)

Note: The PWM2 Cycle Register is shared with Timer2. Therefore, once the user uses the PWM2 resource, the Timer2 Timer/Counter Value can no longer be changed; otherwise, the PWM period output will be abnormal!

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	PWMPDL2[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7 ~ 0	**PWMPDX[15:0]**	PWMn Period Setting This value represents the output waveform period of PWMn minus 1; That is, the period value output by PWMn is: (PWMPDX[15:0] + 1)* PWM Clock

PWM duty is set using the following registers:

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PWM2 Duty Cycle Adjustment Register (R/W)

Address	7	6	5	4	3	2	1	0	Power-On Initial Value
420H	PDT20[15:8]								00000000b
421H	PDT20[7:0]								00000000b
422H	PDT21[15:8]								00000000b
423H	PDT21[7:0]								00000000b

Bit Number	Bit Symbol	Description
7 ~ 0	**PDT20[15:0]**	PWM20 duty cycle setting The High-Level Width of the PWM20 waveform is: (PDT20[15:0] + 1) PWM Clocks
7 ~ 0	**PDT21[15:0]**	PWM21 duty cycle setting The High-Level Width of the PWM21 waveform is: (PDT21[15:0] + 1) PWM Clocks

13.2 PWM2 duty cycle update behavior

When PWM2 outputs a waveform, its duty cycle can be changed by changing the value of the High-Level Setting Register PDTx (x=0 to 1). Note: Changing the PDTx value does not immediately affect the duty cycle; the change takes effect at the start of the next cycle.

13.3 PWM2 period update behavior

When PWM2 outputs a waveform, its Period can be changed by modifying the values in the Period setting Register pair TL2 and TH2. The PWM output Period changes as follows when the Period Register value is changed:

Define the current Period Count Value as Tn, the Timer Count Value when the Period Register is written as Tm, and the Period Count Value to be updated as Tx. Then:

Tm ≤ Tx: The Period changes to Tx in real time

Tm > Tx: The Period change is divided into two stages. In the first stage, after the Period Register is written, the Period Counter increments from its current Count Value until Overflow clears it. In the second stage, the Period changes to Tx.

Preliminary

14 Multi-function pulse width modulation counter PWM0

The SC92R425B provides 10 PWM channels, divided into two categories:

1. Multifunction PWM: 8 channels per group, namely PWM0, with output ports PWM00 to 07.
2. General-Purpose PWM: 2 outputs per group, namely PWM2; output signals: PWM20 to PWM21.

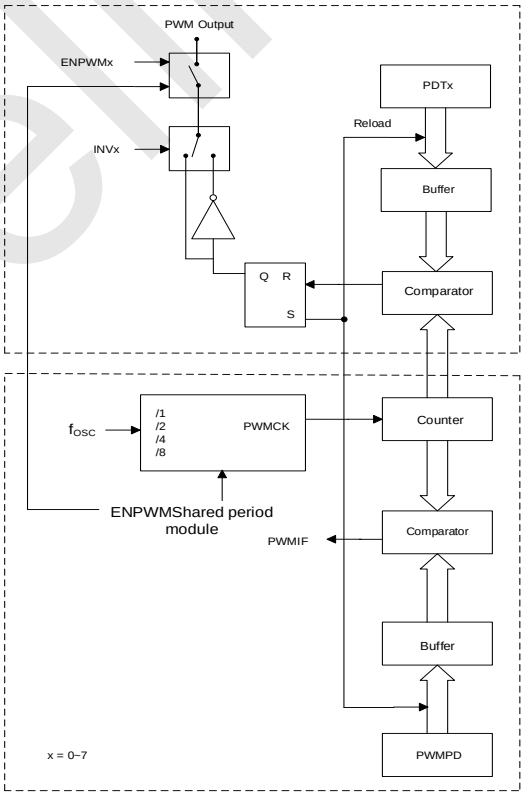
Note: The PWM2 Cycle Register shares TL2 and TH2 with Timer2. Therefore, once PWM2 is in use, do not change the Timer/Counter Value of Timer2; otherwise, the PWM period output will be abnormal!

The SC92R425B PWM0 has the following features:

1. 16-bit PWM resolution.
2. Output waveform can be reversed.
3. Type: center-aligned or edge-aligned.
4. Mode: independent mode or complementary mode.
    1) In Independent mode, all 8 PWM outputs have the same PWM period, but the duty cycle of each PWM output waveform can be set independently.
    2) In complementary mode, four pairs of complementary PWM waveforms with dead time can be output simultaneously.
5. One PWM Overflow Interrupt is provided.
6. Supports a fault detection mechanism.

The SC92R425B PWM0 supports adjustment of the period and duty cycle. The PWMCFG, PWMCON0, and PWMCON1 registers control the PWM status and period, while the output enable state and duty cycle of each PWM channel can be adjusted individually.

14.1 PWM0 block diagram



SC92R425B PWM block diagram

Preliminary

14.2 PWM0 general configuration register

14.2.1 PWM0 general configuration register

The user can set the SC92R425B PWM0 output mode to Independent mode or complementary mode by setting PWMMD[1:0]. In Independent mode, all eight PWM channels have the same period, but the duty cycle of each PWM output waveform can be set individually. In complementary mode, four pairs of complementary PWM waveforms with dead time can be output simultaneously.

The PWM types of the SC92R425B are Edge-Aligned Mode and center-aligned type.

14.2.1.1 Edge-Aligned mode

The PWM Counter counts upward from 0. When the Count Value matches the value in the Duty cycle setting PDTx [15:0], the PWM output changes state. The PWM Counter then continues counting upward until it matches the value of the Period setting PWMPD[15:0] +1 (the end of one PWM period). The PWM Counter is cleared, and a PWM interrupt is generated at this time if the PWM interrupt is enabled. The PWM output waveform is left edge-aligned.

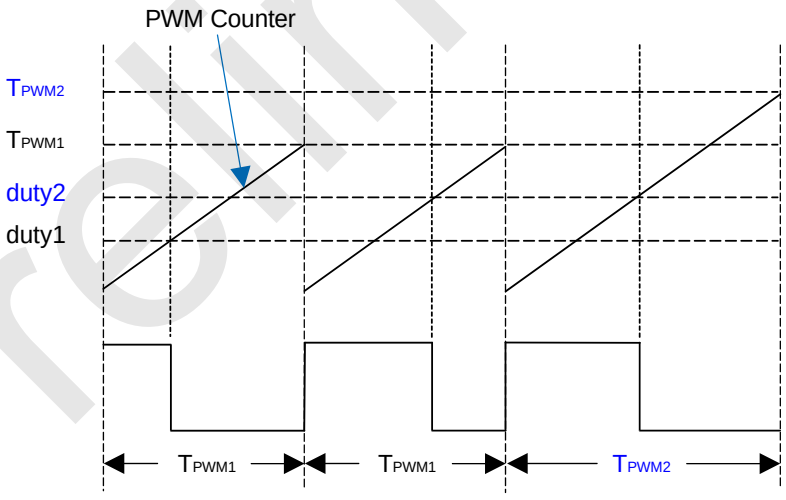
Edge-Aligned Period TPWM Calculation Formula:

$$\mathrm{Tpwm} = \frac{\mathrm{PWMPD}[15:0] + 1}{\mathrm{f_{PWMCK}}}$$

Edge-Aligned Duty cycle Calculation Formula:

$$\mathrm{duty} = \frac{\mathrm{PDTx}\ [15:0]}{\mathrm{PWMPD}[15:0] + 1}$$

Edge-Aligned Waveform Diagram:



Edge-aligned PWM

14.2.1.2 center-aligned type

The PWM Counter counts up from 0. When the Count Value matches the Duty cycle setting PDTx [15:0], the PWM output changes state. The PWM Counter then continues counting up. When the Count Value matches the Period setting PWMPD[15:0] +1 (that is, the midpoint of the PWM period), it automatically starts counting down. When the Count Value matches PDTx [15:0] again, the PWM output changes state again. The PWM Counter then counts down to 0 (underflow), marking the end of one PWM period. If the PWM interrupt is enabled, a PWM interrupt is generated at this point.

Center-aligned type Period TPWM calculation formula:

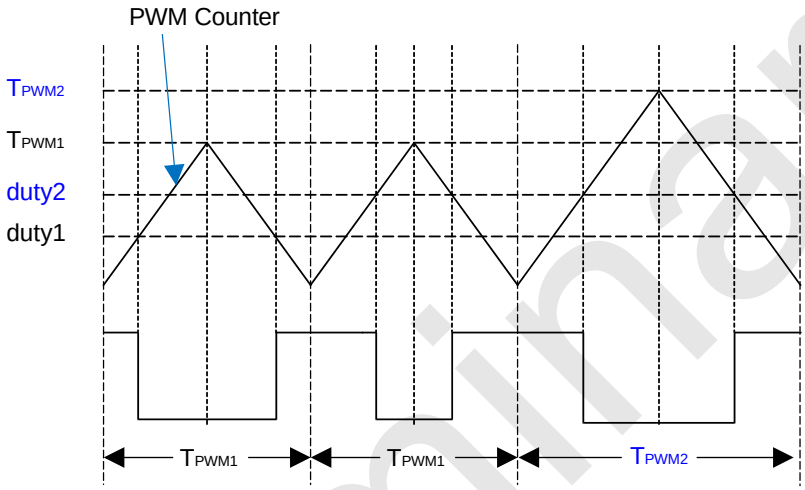
Preliminary

$$Tpwm = 2 * \frac{PWMPD[15:0] + 1}{f_{PWMCK}}$$

Center-aligned Duty cycle calculation formula:

$$duty = \frac{PDTx\ [15:0]}{PWMPD[15:0] + 1}$$

The center-aligned waveform is shown below:



Center-aligned PWM

The above modes and types can be configured through the PWMCON0 Register:

PWMCON0 (D2H) PWM0 Control Register 0 (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	ENPWM	PWMIF	PWMCK[1:0]		-	-	PWMMD[1:0]	
Read/Write	R/W	R/W	R/W	R/W	-	-	R/W	R/W
Power-On Initial Value	0	0	0	0	x	x	0	0

Bit Number	Bit Symbol	Description
7	**ENPWM**	PWM0 module enable control (Enable PWM) 1: Enables the Clock to the PWM0 unit. PWM0 is in operational state, and the state of the PWM0 Output ports is controlled by the ENPWMx Register (x=0 to 7) 0: PWM0 stops working, the PWM0 Counter is cleared, and all PWM0 Output ports are set to GPIO mode
6	**PWMIF**	PWM0 Interrupt Request Flag (PWM Interrupt Flag) When the PWM0 Counter overflows (that is, when the count exceeds PWMPD), this bit is automatically set to 1 by Hardware. If IE1[1] (EPWM) is also set to 1 at this time, a PWM0 interrupt is generated. After a PWM0 interrupt occurs, this bit is not automatically cleared by hardware and must be cleared by software.
5 ~ 4	**PWMCK[1:0]**	PWM0Clock (PWM0 Clock Source Selector) 00:f_{osc} 01:f_{osc}/2 10:f_{osc}/4

Preliminary

Bit Number	Bit Symbol	Description
		11:f_{OSC}/8 For the definition of f_{OSC}, see the block diagram in Section 7.4, High-Frequency System Clock Circuit.
1 ~ 0	**PWMMD[1:0]**	PWM0 operating mode configuration 0x: Independent mode 1x: complementary mode x0: Edge-aligned mode x1: Center-aligned mode
3 ~ 2	**-**	Reserved

PWMCFG (D1H) PWM0 setting Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	INV7	INV6	INV5	INV4	INV3	INV2	INV1	INV0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7 ~ 0	**INVx (x=0 to 7)**	PWM0x waveform output Reverse control 1: PWM0x waveform output Reverse 0: PWM0x waveform output not Reverse

PWMCON1 (D3H) PWM0 control Register 1 (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	EPWM7	EPWM6	EPWM5	EPWM4	EPWM3	EPWM2	EPWM1	EPWM0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7 ~ 0	**ENPWMx (x=0 to 7)**	PWM0x waveform output selection 0: PWM0x output is disabled and configured as a GPIO port 1: When ENPWM=1, the I/O pin for PWM0x functions as a waveform output port

Note:If ENPWM is set to 1, the PWM0 module is enabled, but if ENPWMx=0, PWM0 output is disabled and configured as a GPIO port. At this time, the PWM0 module can be used as a 16-bit Timer. EPWM (IE1.1) is set to 1, and PWM0 will still generate an Interrupt.

PWMPDL (D4H) Period Register Lower 8 Bits (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	PWMPDL[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

PWMPDH (D5H) Period Register High 8 Bits (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	PWMPDH[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Preliminary

Bit Number	Bit Symbol	Description
7 ~ 0	**PWMPD[15:0]**	Period setting shared by PWM0 This value represents the PWM0 output waveform's (Period - 1); In other words, the Period value output by PWM0 is (PWMPD[15:0] + 1) * PWM Clock

IE1 (A9H) Interrupt Enable Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	-	-	-	ETK	-	EBTM	EPWM	ESSI
Read/Write	-	-	-	R/W	-	R/W	R/W	R/W
Power-On Initial Value	x	x	x	0	x	0	0	0

Bit Number	Bit Symbol	Description
1	**EPWM**	PWM0 interrupt Enable bit 0: Disable the PWM0 interrupt 1: Interrupt generation on PWM0 Counter Overflow enabled

IP1 (B9H) Interrupt Priority Control Register 1 (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	-	-	-	IPTK	-	IPBTM	IPPWM	IPSSI
Read/Write	-	-	-	R/W	-	R/W	R/W	R/W
Power-On Initial Value	x	x	x	0	x	0	0	0

Bit Number	Bit Symbol	Description
1	**IPPWM**	PWM0 interrupt priority selection 0: Set the PWM0 interrupt priority to "Low" 1: Set the PWM0 interrupt priority to "High"

14.2.2 PWM0 fault detection function configuration

Fault detection is commonly used for motor system protection. When the Fault Detection Function is enabled, setting FLTEN1 (PWMFLT.7) to 1 enables the fault detection signal input pin (FLT). When the signal on the FLT pin meets the fault condition, the FLTSTA1 Flag is set to 1 by Hardware, and the PWM0 output stops. The PWM0 Counter continues counting, and the PWM0 interrupt is unaffected. The Fault Detection Mode can be set to Latch Mode or Immediate Mode; In Immediate Mode, when the fault signal on the FLT pin meets the deactivation condition, the FLTSTA1 Flag is cleared by Hardware. The PWM0 Counter continues counting until it reaches zero, after which the PWM0 output resumes; In Latch Mode, when the fault signal on the FLT Pin meets the disable condition, the status of the FLTSTA1 Flag remains unchanged. The user can clear it by software. Once the FLTSTA1 status is cleared, the PWM0 Counter continues counting until it reaches zero, after which PWM0 resumes output. The Fault Detection Mode is divided into Latch Mode and Immediate Mode. The specific configuration is as follows:

PWMFLT (D7H) PWM Fault Detection Configuration Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	FLTEN1	FLTSTA1	FLTMD1	FLTLV1	-	-	FLTDT1[1:0]	
Read/Write	R/W	Read/write	R/W	R/W	-	-	R/W	R/W
Power-On Initial Value	0	0	0	0	x	x	0	0

Bit Number	Bit Symbol	Description
7	**FLTEN1**	PWM0 Fault Detection Function Control Bit 0: Fault Detection Function disabled

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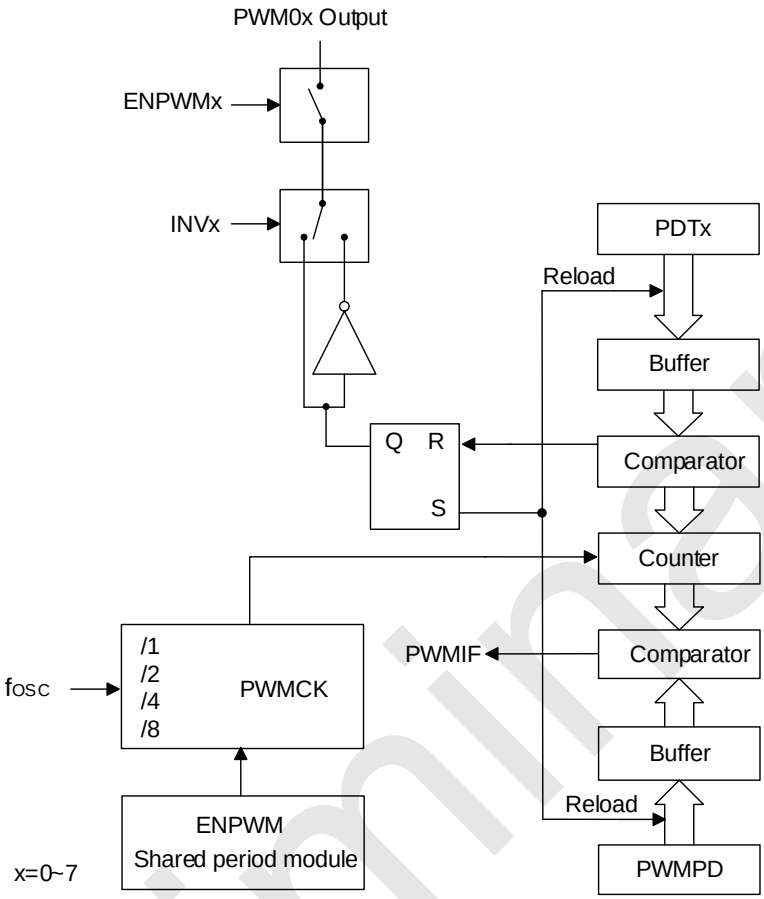
Bit Number	Bit Symbol	Description
		1: Fault Detection Function enabled
6	**FLTSTA1**	PWM0 Fault Detection Status Flag 0: PWM0 operates normally 1: Fault detection is active; PWM0 output is in a high-impedance state. In Latch Mode, this bit can be cleared to 0 by software
5	**FLTMD1**	PWM0 Fault Detection Mode setting bit 0: Latch Mode. When the Fault Input is active, FLTSTA1 is set to "1" and PWM0 stops outputting. When the Fault Input is inactive, the state of FLTSTA1 remains unchanged 1: Immediate Mode: When the Fault Input is active, FLTSTA1 is set to "1" and PWM0 stops outputting. When the Fault Input is inactive, FLTSTA1 is immediately cleared to 0, and the PWM0 waveform resumes output when the PWM0 time-base counter reaches zero
4	**FLTLV1**	PWM0 Fault Detection Level selection bit 0: Fault Detection active low 1: Fault Detection active high
1 ~ 0	**FLTDT1[1:0]**	PWM0 Fault Detection input signal Filtering Time setting 00: Filtering Time is 0 01: Filtering Time is 1 μs 10: Filtering Time is 4 μs 11: Filtering Time is 16 μs
3 ~ 2	**-**	Reserved

14.3 Independent mode

In Independent mode (PWMMD.1= 0), the Duty cycle of each of the 8 PWM Channels can be set independently. After configuring the PWM output states and Period, the user can configure the Duty Cycle Register for the corresponding PWM Channel to output a PWM waveform at a fixed Duty cycle.

14.3.1 PWM0 independent mode block diagram

Preliminary



SC92R425B PWM independent mode block diagram

14.3.2 PWM0 independent mode duty cycle configuration

PWM0 Duty Cycle Adjustment Register PDTx (R/W)

Address	7	6	5	4	3	2	1	0	Power-On Initial Value
418H	PDT00[15:8]								00000000b
419H	PDT00[7:0]								00000000b
41AH	PDT01[15:8]								00000000b
41BH	PDT01[7:0]								00000000b
41CH	PDT02[15:8]								00000000b
41DH	PDT02[7:0]								00000000b
41EH	PDT03[15:8]								00000000b
41FH	PDT03[7:0]								00000000b
408H	PDT07[15:8]								00000000b
409H	PDT07[7:0]								00000000b
40AH	PDT06[15:8]								00000000b
40BH	PDT06[7:0]								00000000b
40CH	PDT05[15:8]								00000000b

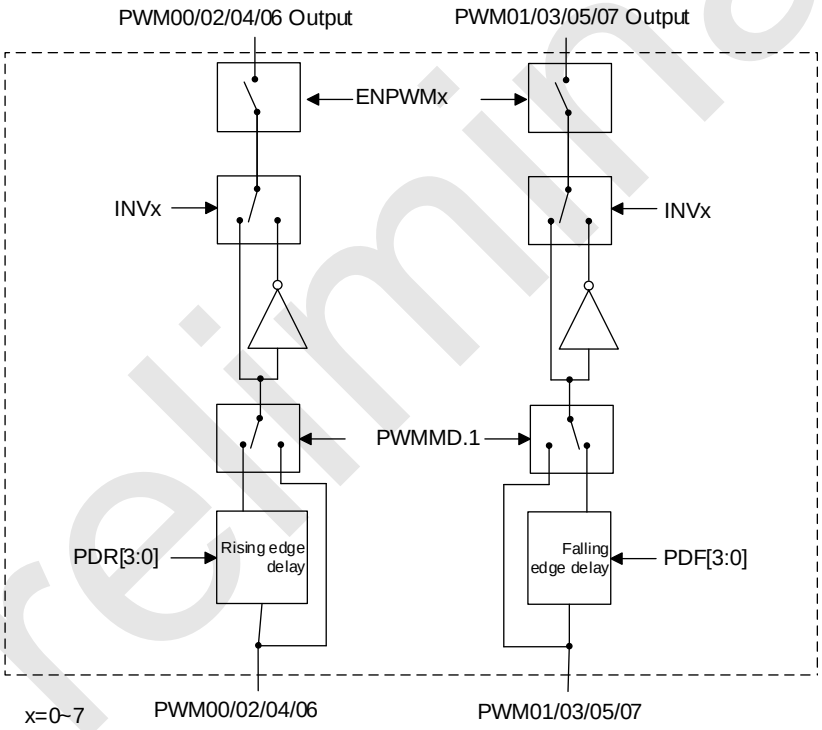
Preliminary

Address	7	6	5	4	3	2	1	0	Power-On Initial Value
40DH	PDT05[7:0]								00000000b
40EH	PDT04[15:8]								00000000b
40FH	PDT04[7:0]								00000000b

Bit Number	Bit Symbol	Description
15 ~ 0	**PDTx [15:0] (x=0 to 7)**	PWM0x waveform duty cycle setting The High-Level Width of the PWM0x waveform is (PDTx [15:0]) PWM Clocks

14.4 Complementary mode

14.4.1 PWM0 complementary mode Block Diagram



SC92R425B PWM complementary mode block diagram

14.4.2 PWM0 Complementary-Mode Duty Cycle Configuration

In complementary mode (PWMMD[1:0] = 1x), PWM00/PWM01, PWM02/PWM03, PWM04/PWM05, and PWM06/PWM07 are divided into four pairs, with the duty cycle of each pair adjusted by PDT0[15:0], PDT2[15:0], PDT4[15:0], and PDT6[15:0], respectively

Registers PDT1[15:0], PDT3[15:0], PDT5[15:0], and PDT7[15:0] are invalid in complementary mode.

PWM0 Duty Cycle Adjustment Register PDTx (R/W)

Address	7	6	5	4	3	2	1	0	Power-On Initial Value
418H	PDT00[15:8]								00000000b
419H	PDT00[7:0]								00000000b

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Address	7	6	5	4	3	2	1	0	Power-On Initial Value
41AH	PDT01[15:8]								00000000b
41BH	PDT01[7:0]								00000000b
41CH	PDT02[15:8]								00000000b
41DH	PDT02[7:0]								00000000b
41EH	PDT03[15:8]								00000000b
41FH	PDT03[7:0]								00000000b
408H	PDT07[15:8]								00000000b
409H	PDT07[7:0]								00000000b
40AH	PDT06[15:8]								00000000b
40BH	PDT06[7:0]								00000000b
40CH	PDT05[15:8]								00000000b
40DH	PDT05[7:0]								00000000b
40EH	PDT04[15:8]								00000000b
40FH	PDT04[7:0]								00000000b

Bit Number	Bit Symbol	Description
15 ~ 0	**PDTx [15:0] (x=0, 2, 4, 6)**	PWM waveform duty cycle setting for PWMx and PWMy pins (y=x+1) The High-Level Width of the PWM waveforms on Pins Px and Py is (PDTx [15:0]) PWM Clocks

14.4.3 PWM0 complementary mode Dead Time Setting

When the SC92R425B PWM0 operates in complementary mode, the dead zone control module prevents overlap between the two complementary PWM output signals, ensuring that the pair of complementary power switches driven by the PWM signals do not conduct simultaneously.

PWMDFR (D6H) PWM0 Dead Time Setting Register (R/W)

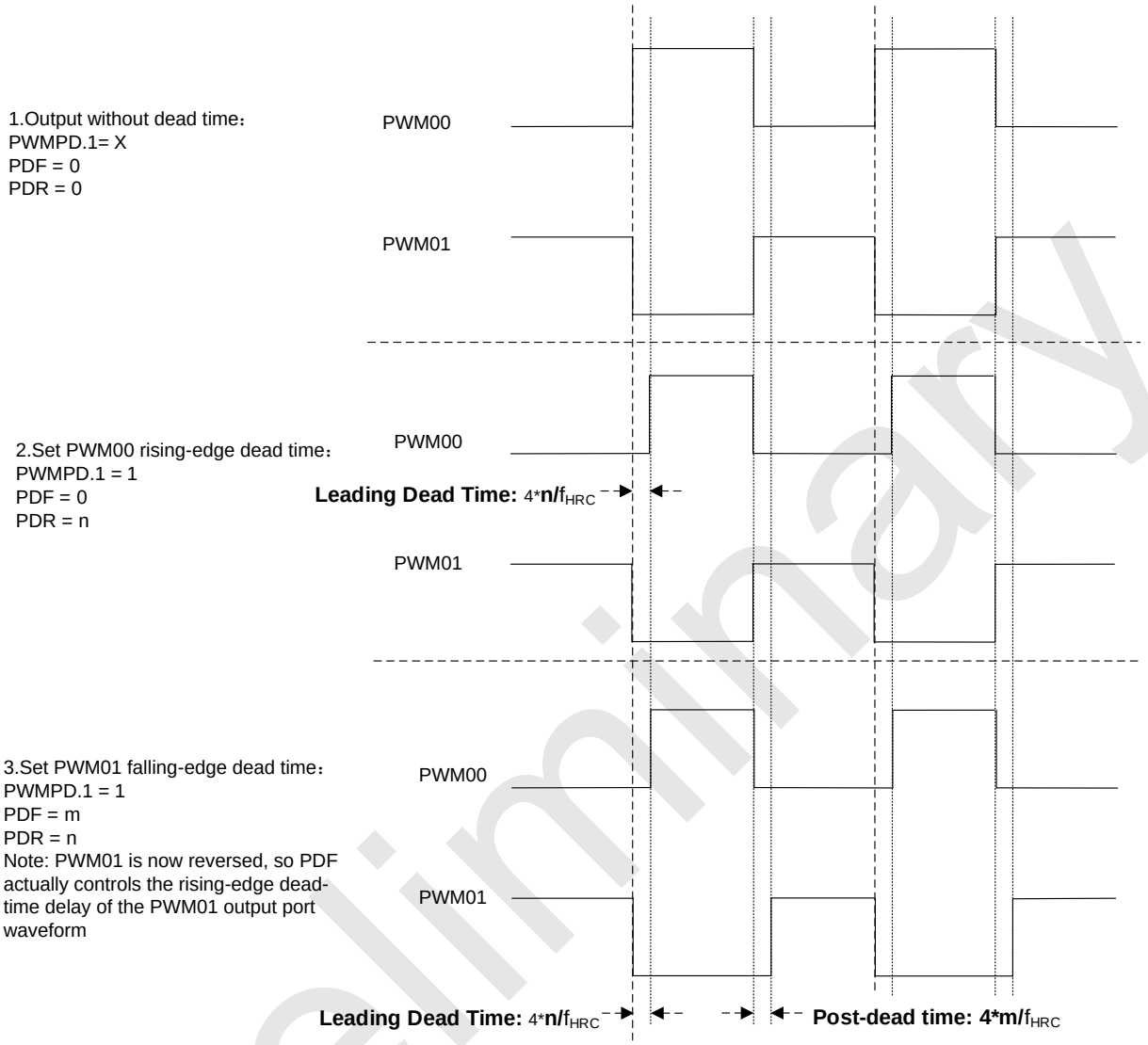
Bit Number	7	6	5	4	3	2	1	0
Symbol	**PDF[3:0]**				**PDR[3:0]**			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7 ~ 4	**PDF[3:0]**	complementary mode: PWM Falling-edge dead time = 4*PDF[3:0] / f_{PWMCK}
3 ~ 0	**PDR[3:0]**	complementary mode: PWM Rising-edge dead time = 4*PDR[3:0] / f_{PWMCK}

14.4.4 PWM dead-time output waveform

The diagram below shows the dead-time adjustment waveform for PWM00 and PWM01 in complementary mode. For clarity, PWM01 is shown inverted (INV1=1).

Preliminary



PWM dead-time output waveform

14.5 PWM0 waveform and usage

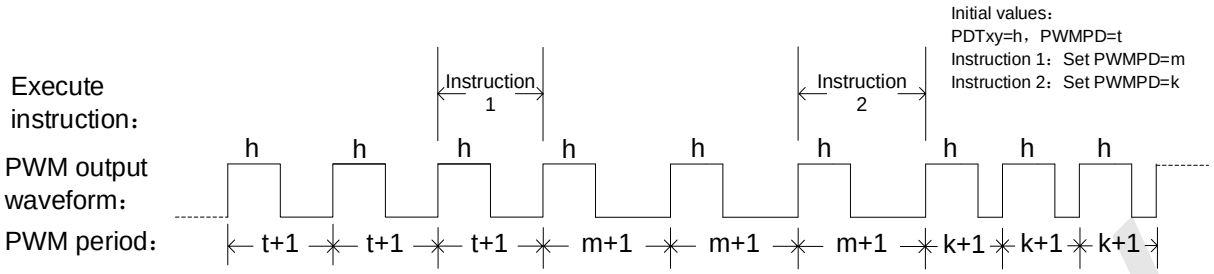
The effects of changes to each SFR parameter on the PWM0 waveform are described below:

1. Duty cycle update behavior

When PWMn outputs a waveform, the duty cycle can be changed by changing the value of the High-Level Setting Register (PDTx). However, note that changing the PDTx value does not immediately affect the duty cycle; the change takes effect at the start of the next period.

2. Period update behavior

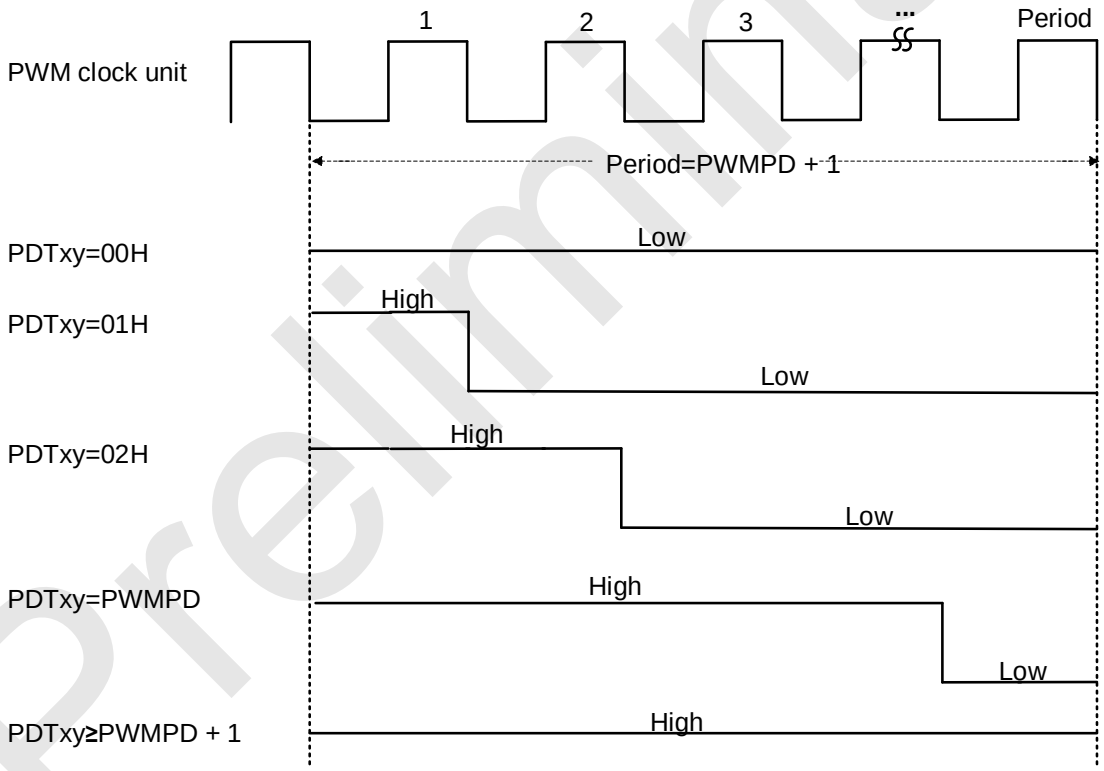
Preliminary



Period update behavior diagram

When PWM0 outputs a waveform, the period can be changed by changing the value of the period setting register PWMPD. Changing the value of PWMPD does not change the period immediately; the change takes effect in the next cycle, after the current cycle ends, as shown in the figure above.

3. Relationship Between Period and Duty Cycle



The relationship between period and duty cycle

The relationship between the Period and Duty cycle is shown in the figure above. This result assumes that the PWM0 output Reverse control (INV0x, x=0 to 7) is initially 0; to obtain the opposite result, set INV0x to 1.

Preliminary

15 GP I/O

The SC92R425B provides 26 controllable bidirectional GPIO ports. The input/output Control Register controls the input/output status of each port. When configured as inputs, the I/O ports each have an internal Pull-up resistor controlled by PxPHy. These 26 IO ports are multiplexed with other functions. Whether an I/O port is configured as an input or an output, reading its Data Register returns the port's actual state.

Note: Unused and packaged I/O ports that are not exposed must be configured as Strong Push-Pull Output Mode.

15.1 GPIO structure diagram

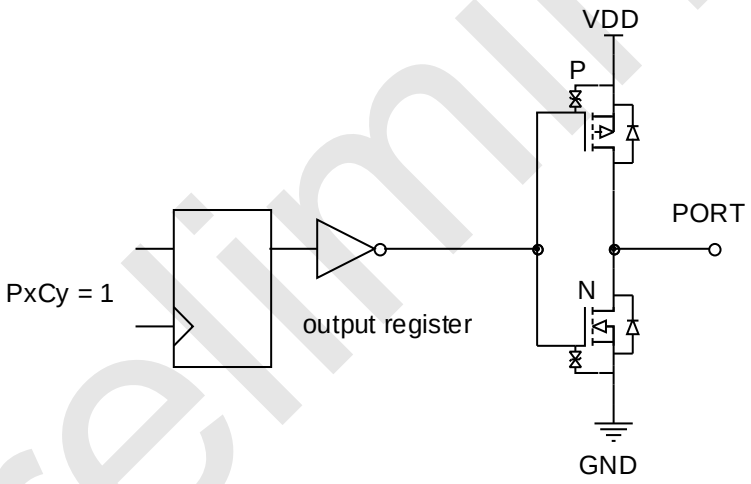
15.1.1 Strong push-pull output mode

In Strong Push-Pull Output Mode, the port can provide sustained high-current drive:

P00 to P03, P10 to P13, P50, and P51 support a high-level output of 15 mA@4.3 V and a low-level output of 70 mA@0.8 V.

P04 to P07, P14 to P17, and P20 to P27 support a high-level output of 20 mA@4.3 V and a low-level output of 150 mA@0.8 V.

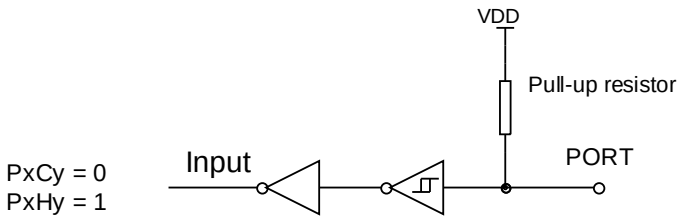
The port structure diagram for Strong Push-Pull Output Mode is shown below:



Strong push-pull output mode

15.1.2 Input mode with pull-up

In Input Mode with Pull-up, a pull-up resistor is permanently connected to the input port. A low-level signal is detected only when the input port is pulled low. The port structure diagram for Input Mode with Pull-up is shown below:

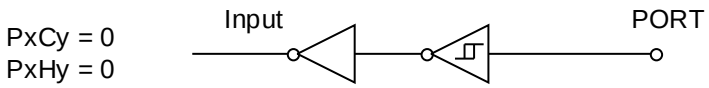


Preliminary

Input mode with pull-up

15.1.3 High-impedance input mode (Input only)

The port structure diagram for High-impedance input mode is shown below:



High-impedance input mode

15.2 I/O port-related registers

P0CON (9AH)P0 Port Input/Output Control Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	P0C7	P0C6	P0C5	P0C4	P0C3	P0C2	P0C1	P0C0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

P0PH (9BH)P0 Port Pull-Up Resistor Control Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	P0H7	P0H6	P0H5	P0H4	P0H3	P0H2	P0H1	P0H0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

P1CON (91H)P1 Port Input/Output Control Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	P1C7	P1C6	P1C5	P1C4	P1C3	P1C2	P1C1	P1C0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

P1PH (92H)P1 Port Pull-Up Resistor Control Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	P1H7	P1H6	P1H5	P1H4	P1H3	P1H2	P1H1	P1H0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

P2CON (A1H)P2 Port Input/Output Control Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	P2C7	P2C6	P2C5	P2C4	P2C3	P2C2	P2C1	P2C0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On	0	0	0	0	0	0	0	0

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Bit Number	7	6	5	4	3	2	1	0
Initial Value								

P2PH (A2H)P2 Port Pull-Up Resistor Control Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	P2H7	P2H6	P2H5	P2H4	P2H3	P2H2	P2H1	P2H0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

P5CON (D9H)P5 Port Input/Output Control Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	P5C1	P5C0
Read/Write	-	-	-	-	-	-	R/W	R/W
Power-On Initial Value	x	x	x	x	x	x	0	0

P5PH (DAH)P5 Port Pull-Up Resistor Control Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	P5H1	P5H0
Read/Write	-	-	-	-	-	-	R/W	R/W
Power-On Initial Value	x	x	x	x	x	x	0	0

Bit Number	Bit Symbol	Description
7 ~ 0	**PxCy** **(x=0 to 2, 5, y=0 to 7)**	Port Px input/output control: 0: Pxy is in Input mode (Power-On Initial Value) 1: Pxy is in Strong Push-Pull Output Mode
7 ~ 0	**PxHy** **(x=0 to 2, 5, y=0 to 7)**	Port Px Pull-up resistor setting, effective only when PxCy=0: 0: Pxy is in High-impedance input mode (Power-On Initial Value), Pull-up resistor disabled 1: Pull-up resistor enabled for Pxy

P0 (80H) Port P0 Data Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

P1 (90H) Port P1 Data Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

P2 (A0H) Port P2 Data Register (R/W)

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Bit Number	7	6	5	4	3	2	1	0
Symbol	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

P5 (D8H) Port P5 Data Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	P5.1	P5.0
Read/Write	-	-	-	-	-	-	R/W	R/W
Power-On Initial Value	x	x	x	x	x	x	0	0

Bit Number	Bit Symbol	Description
7 ~ 0	**P0.x (x=0 to 7)**	Port P0 Latch Register Data
7 ~ 0	**P1.x (x=0 to 7)**	Port P1 Latch Register Data
7 ~ 0	**P2.x (x=0 to 7)**	Port P2 Latch Register Data
7 ~ 0	**P3.x (x=0 to 7)**	Port P3 Latch Register Data
7 ~ 0	**P4.x (x=0 to 7)**	Port P4 Latch Register Data
1 ~ 0	**P5.x (x=0 to 1)**	Port P5 Latch Register Data

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16 UART0

The SC92R425B supports one full-duplex serial port for convenient connection to other devices, such as a Wi-Fi module circuit or a driver chip for another UART communication interface. The functions and features of UART0 are as follows:

1. Three communication modes are available: Mode 0, Mode 1, and Mode 3
2. Timer 1 or Timer 2 can be selected as the baud rate generator
3. Interrupts RI/TI are generated upon completion of transmission and reception; the interrupt flags must be cleared by software.

UART0 pins TXD0 and RXD0 can be mapped to any pin; see PORT Mapped Register (R/W)

SCON (98H) Serial Port Control Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7 ~ 6	**SM0 to 1**	Serial Communication Mode Control Bit 00: Mode 0, 8-bit half-duplex synchronous communication mode; serial data is received and transmitted on the RXD pin. The TXD pin is used as the transmit shift clock. Each frame receives or transmits 8 bits, with the low-order bit first 01: Mode 1, 10-bit full-duplex asynchronous communication, consisting of 1 Start Bit, 8 Data Bits, and 1 Stop Bit; the communication baud rate is variable 10: Reserved 11: Mode 3, 11-bit full-duplex asynchronous communication, consisting of 1 Start Bit, 8 Data Bits, one Programmable 9th Bit, and 1 Stop Bit; the communication baud rate is variable.
5	**SM2**	Serial Communication Mode Control Bit 2; this Control Bit is valid only in Mode 3 0: RI is set and an Interrupt Request is generated each time a complete Data Frame is received 1: When a complete Data Frame is received, RI is set and an Interrupt Request is generated only when RB8=1.
4	**REN**	Receive Enable Control Bit 0: Data reception is disabled 1: Data reception is enabled.
3	**TB8**	Valid only in Mode 3; this is the 9th Bit of Transmitted Data
2	**RB8**	Valid only in Mode 3; this is the 9th Bit of Received Data
1	**TI**	Transmit Interrupt flag After transmission is complete, this bit is set to 1 by Hardware and must be cleared to 0 by user software
0	**RI**	Receive Interrupt flag After reception is complete, this bit is set to 1 by Hardware and must be cleared to 0 by user software

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SBUF (99H) Serial Port Data Buffer Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	SBUF[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7 ~ 0	**SBUF[7:0]**	**Serial Port Data Buffer Register** SBUF contains two registers: a Transmit Shift Register and a Receive Latch. Data written to SBUF is sent to the Transmit Shift Register and starts the transmission process; reading SBUF returns the contents of the Receive Latch.

PCON (87H) Power Management Control Register (W, *not readable *)

Bit Number	7	6	5	4	3	2	1	0
Symbol	SMOD	-	LDLOCK	-	RST	-	STOP	IDL
Read/Write	W	-	R/W	-	W	-	W	W
Power-On Initial Value	0	x	0	x	n	x	0	0

Bit Number	Bit Symbol	Description
7	**SMOD**	● When SM0 to 1 = 01 (UART0 mode 1) or SM0 to 1 = 11 (UART0 mode 3), baud rate multiplier setting bit: ■ 0: Serial port operates with the system clock divided by 1 ■ 1: Serial port operates with the system clock divided by 16 ● When SM0 to 1 = 00 (UART0 mode 0), baud rate multiplier setting bit: ■ 0: Serial port operates with the system clock divided by 12 ■ 1: Serial port operates with the system clock divided by 4

16.1 Baud rate for serial port communication

In mode 0, the Serial port clock source can be programmed to the system clock divided by 12 or 4, as determined by the SMOD (PCON.7) bit. When SMOD is 0, the Serial port operates with the system clock divided by 12. When SMOD is 1, the serial port operates with the system clock divided by 4.

In Modes 1 and 3, the serial port clock source can be programmed to use the system clock divided by 1 or 16, as determined by the SMOD (PCON.7) bit. When SMOD is 0, the serial port operates with the system clock divided by 1. When SMOD is 1, the serial port operates with the system clock divided by 16. Once the serial port clock source is determined, the baud rate overflow rate is set by Timer 1 or Timer 2:

- When both the TCLK (T2CON.4) and RCLK (T2CON.5) bits are 0, Timer 1 operates in baud rate generator mode, and the UART0 baud rate overflow rate is set by [TH1,TL1]. The formula is as follows. Note: When Timer 1 is used as the Baud rate generator, Timer 1 must stop counting, i.e., TR1=0:
  - SMOD = 0: $\mathrm{BaudRate} = \frac{f_{SYS}}{[TH1,TL1]}$; (Note: [TH1,TL1] must be greater than 0x0010)
  - SMOD = 1:$\mathrm{BaudRate} = \frac{1}{16} * \frac{f_{SYS}}{[TH1,TL1]}$
- When either TCLK (T2CON.4) or RCLK (T2CON.5) is 1, Timer 2 operates in Baud rate generator mode, and the UART0 Baud Rate Overflow Rate is set by [RCAP2H, RCAP2L], as follows:

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- SMOD = 0: $\text{BaudRate} = \frac{f_{SYS}}{[\text{RCAP2H,RCAP2L}]}$; (Note: [RCAP2H,RCAP2L] must be greater than 0x0010)
- SMOD = 1:$\text{BaudRate} = \frac{1}{16} * \frac{f_{SYS}}{[\text{RCAP2H,RCAP2L}]}$

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17 SPI/TWI/UART three-in-one serial interface (SSI)

The SC92R425B integrates a three-in-one serial communication interface configurable as UART, SPI, or TWI (SSI), facilitating connections between the MCU and devices with different interfaces. The user can configure the SSI interface to any one of the SPI, TWI, and UART communication modes by setting the SSMOD[1:0] bits in the OTCON register. Its features are as follows:

1. SPI mode can be configured for either Master mode or Slave Mode.
2. In TWI mode, communication is limited to Slave Mode.
3. UART mode can operate in Mode 1 (10-bit Full-Duplex Asynchronous Communication) or Mode 3 (11-bit Full-Duplex Asynchronous Communication).
4. SSI pins SSICK0, SSITX0, and SSIRX0 can be mapped to any pin; see the PORT Mapped Register (R/W).

The specific configuration method is as follows:

OTCON (8FH) Output Control Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	SSMOD[1:0]		-	-	-	-	-	-
Read/Write	R/W	R/W	-	-	-	-	-	-
Power-On Initial Value	0	0	x	x	x	x	x	x

Bit Number	Bit Symbol	Description
7 ~ 6	**SSMOD[1:0]**	**SSI Communication Mode Control Bit** 00: SSI disabled 01: SSI set to SPI Communication Mode 10: SSI set to TWI Communication Mode 11: SSI set to UART Communication Mode

17.1 SPI

SSMOD[1:0] = 01, the One-of-three serial interface SSI is configured as an SPI interface. The Serial Peripheral Interface (SPI) is a high-speed serial Communication interface that allows the MCU to perform Full duplex, synchronous serial Communication with peripherals (including other MCUs).

17.1.1 Registers related to SPI operations

SSCON0 (9DH) SPI Control Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	SPEN	-	MSTR	CPOL	CPHA	SPR2	SPR1	SPR0
Read/Write	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	x	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7	**SPEN**	**SPI Enable Control** 0: SPI disabled 1: SPI enabled
5	**MSTR**	**SPI Master/Slave Selection** 0: SPI is a Slave device 1: SPI is a Master device
4	**CPOL**	**Clock Polarity Control Bit** 0: SCK is Low level in the Idle State

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Bit Number	Bit Symbol	Description
		1: SCK is High level in the Idle State
3	**CPHA**	**Clock Phase Control Bit** 0: Data is sampled on the first edge of the SCK Period 1: Data is sampled on the second edge of the SCK Period
2 ~ 0	**SPR[2:0]**	**SPI Clock Rate Selection Bit** 000: f_{SYS} /4 001: f_{SYS} /8 010: f_{SYS} /16 011:f_{SYS} /32 100:f_{SYS} /64 101:f_{SYS} /128 110:f_{SYS} /256 111:f_{SYS} /512
6	**-**	Reserved

SSCON1 (9EH)SPI Status Register (R/W)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	SPIF	WCOL	-	-	-	DORD	-	TBIE
Read/Write	R/W	R/W	-	-	-	R/W	-	R/W
Power-On Initial Value	0	0	x	x	x	0	x	0

Bit Number	Bit Symbol	Description
7	**SPIF**	**SPI Data Transfer Flag** 0: Cleared by software 1: Indicates that data transfer is complete; set by Hardware
6	**WCOL**	**Write Collision Flag** 0: Cleared by software, indicating that the write collision has been handled 1: Set by Hardware, indicating that a collision has been detected
2	**DORD**	**Transfer Direction Select Bit** 0: Transmit MSB first 1: Transmit LSB first
0	**TBIE**	**Transmit Buffer Interrupt Enable Control Bit** 0: Interrupt generation is disabled when SPIF=1 1: When SPIF=1, an SPI interrupt is generated
5 ~ 3, 1	**-**	Reserved

SSDAT (9FH) SPI Data Register (R/W)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	SPD[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7 ~ 0	**SPD[7:0]**	**SPI Data Buffer Register** Data written to SSDAT is placed in the Transmit Shift Register.

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Bit Number	Bit Symbol	Description
		Reading SSDAT returns the Data in the Receive Shift Register.

17.1.2 Signal description

Master Out, Slave In (MOSI):

This signal connects the master device to a slave device. Data is serially transmitted from the master device to the slave device via MOSI; the master device outputs data, and the slave device inputs data.

Master In, Slave Out (MISO):

This signal connects the slave device to the master device. Data is serially transmitted from the slave device to the master device via MISO; the slave device outputs data, and the master device inputs data. When the SPI is configured as a slave device and is not selected, the slave device's MISO pin is in a high-impedance state.

SPI Serial Clock (SCK):

The SCK signal is used to control the synchronous transfer of input and output data on the MOSI and MISO lines. One Byte is transferred on the lines every 8 Clock Cycles. If the slave device is not selected, the SCK signal is ignored by that slave device.

17.1.3 Operating mode

The SPI can be configured in either Master mode or Slave Mode. The SPI module is configured and initialized by setting the SSCON0 Register (SPI Control Register) and SSCON1 (SPI Status Register). After configuration is complete, data transfer is performed by setting SSCON0, SSCON1, and SSDAT (SPI Data Register).

During SPI communication, data is synchronously shifted in and out serially. The serial Clock line (SCK) keeps the movement and sampling of data on the two serial Data Lines (MOSI and MISO) synchronized. If a Slave device is not selected, it cannot participate in activity on the SPI bus.

When the SPI master device transmits data to a Slave device over the MOSI line, the Slave device sends data to the master device over the MISO line in response, enabling synchronous Full duplex transmission and reception of data under the same Clock. The Transmit Shift Register and Receive Shift Register share the same Special-Function Unit address. Writing to the SPI Data Register SSDAT writes to the Transmit Shift Register, while reading the SSDAT Register retrieves data from the Receive Shift Register.

Some devices expose an SS pin (Slave device select pin, active low) for their SPI interface. When communicating with the SC92R425B over the SPI bus, the SS pins of other devices on the SPI bus must be connected according to the Communication Mode. The following table lists how the SS pins of other devices on the SPI bus should be connected in each SPI Communication Mode of the SC92R425B:

SC92R425B SPI	Other devices on the SPI bus	Mode	Slave SS (Slave device select pin)
Master mode	Slave mode	One Master, one Slave	Pull low
		One Master, multiple Slaves	The SC92R425B provides multiple I/O pins, each connected to the SS pin of a Slave. Before data transfer, the SS pin of the Slave device must be pulled low
Slave mode	Master mode	One Master, one Slave	Pull high

17.1.3.1 Master mode

- **Mode enabled**

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The SPI master device controls the initiation of all Data Transfers on the SPI bus. When the MSTR bit in the SSCON0 Register is set, the SPI operates in Master mode, and only one Master device can initiate a transfer.

- **Transmit**

In SPI Master mode, writing one byte of data to the SPI Data Register SSDAT writes the data to the Transmit Shift Register. If the Transmit Shift Register already contains data, the Master SPI generates a WCOL signal to indicate that the write was too fast. However, the data in the Transmit Shift Register is not affected, and transmission is not interrupted. Also, if the Transmit Shift Register is not empty, the Master device immediately shifts the data out of the Transmit Shift Register serially onto the MOSI line at the SPI Clock Frequency on SCK. When transmission is complete, the SPIF bit in the SSCON1 Register is set to 1. If the SPI interrupt is enabled, an interrupt is also generated when the SPIF bit is set to 1.

- **Receive**

When the Master device transmits Data to the Slave device over the MOSI line, the corresponding Slave device simultaneously transfers the contents of its Transmit Shift Register to the Master device's Receive Shift Register over the MISO line, enabling Full duplex operation. Therefore, setting the SPIF flag indicates both that transmission is complete and that Received Data has been received. Data received by the Slave device is shifted into the Master device's Receive Shift Register in the selected MSB-first or LSB-first direction. When a Byte of Data has been completely shifted into the Receive Register, the processor can read the Data from the SSDAT Register.

17.1.3.2 Slave mode

- **Mode enabled**

When the MSTR bit in the SSCON0 Register is cleared, the SPI operates in Slave mode.

- **Transmit and Receive**

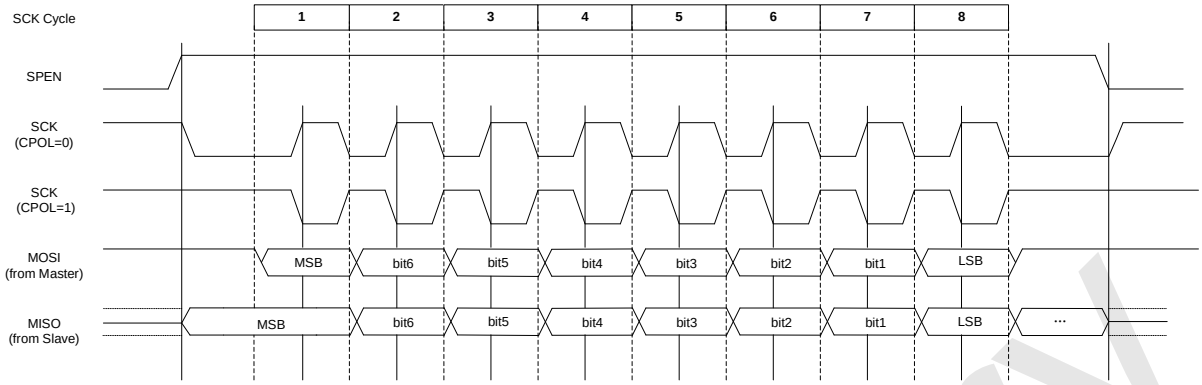
In Slave Mode, Data is shifted in through the MOSI pin and shifted out through the MISO pin according to the SCK signal controlled by the Master device. A Bit Counter records the number of SCK edges. When the Receive Shift Register has shifted in 8 bits of Data (one Byte) and the Transmit Shift Register has shifted out 8 bits of Data (one Byte), the SPIF flag is set to 1. The Data can be obtained by reading the SSDAT Register. If the SPI interrupt is enabled, an interrupt is also generated when SPIF is set to 1. At this point, the Receive Shift Register retains its original Data and the SPIF bit is set to 1, so the SPI Slave device will not receive any Data until SPIF is cleared to 0. The SPI Slave device must Write the Data to be transmitted to the Transmit Shift Register before the Master device starts a new Data Transfer. If no Data is written before transmission starts, the Slave device will transmit the "0x00" Byte to the Master device. If an SSDAT write operation occurs during a transfer, the SPI Slave device sets the WCOL Flag. That is, if the transfer Shift Register already contains data, the SPI Slave device sets WCOL to indicate an SSDAT write collision. However, the data in the Shift Register is not affected, and the transfer is not interrupted.

17.1.4 Transfer modes

By setting the CPOL and CPHA bits in the SSCON0 Register in software, the user can select one of four combinations of SPI Clock polarity and phase. The CPOL bit defines the Clock polarity, i.e., the logic level when idle. It has little effect on the SPI transfer format. The CPHA bit defines the Clock phase, i.e., the Clock edge on which data sampling and shifting are enabled. The clock polarity and phase settings must be consistent between the two devices in master-slave communication.

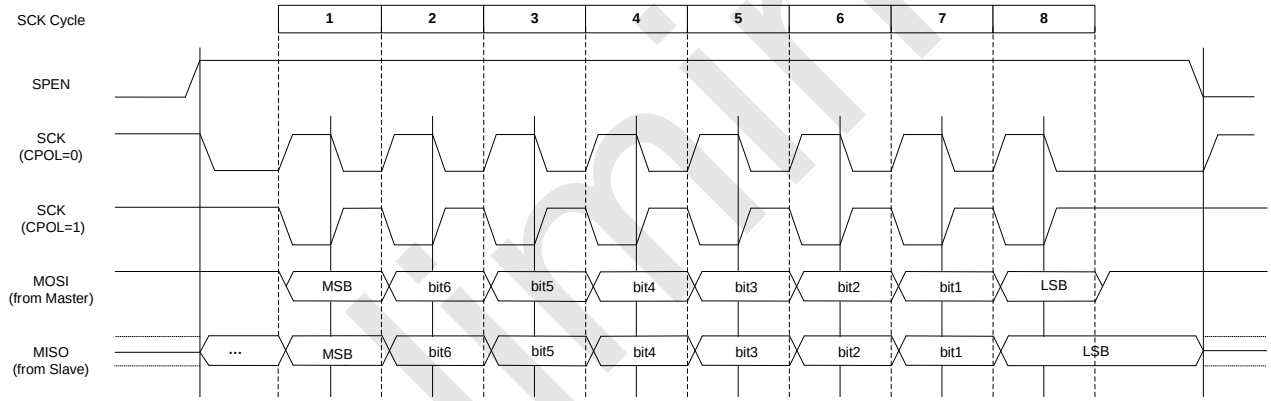
When CPHA = 0, data is captured on the first SCK edge. The slave device must have the data ready before the first SCK edge.

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CPHA = 0 Data Transfer Diagram

When CPHA = 1, the master device outputs data on the MOSI line on the first SCK edge. The slave device uses the first SCK edge as the start of the transmission signal and begins capturing data on the second SCK edge. Therefore, the user must complete the write to SSDAT within the first two SCK edges. This data transfer format is the preferred form of communication between one master device and one slave device.



CPHA = 1 Data Transfer Diagram

17.1.5 Error detection

Writing to the SSDAT Register during a data transmission sequence causes a write collision, and the WCOL bit in the SSCON1 Register is set to 1. Setting the WCOL bit to 1 does not cause an interrupt or abort the transmission. The WCOL bit must be cleared to 0 by software.

17.2 TWI

When SSMOD[1:0] = 10, the One-of-three serial interface SSI is configured as a TWI interface. The SC92R425B can only operate as a Slave during TWI Communication.

SSCON0 (9DH) TWI Control Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	TWEN	TWIF	-	GCA	AA	STATE[2:0]		
Read/Write	R/W	R/W	-	Read	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	x	0	0	0	0	0

Bit Number	Bit Symbol	Description
7	**TWEN**	TWI enable control 0: Disable TWI 1: Enable TWI

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Bit Number	Bit Symbol	Description
6	**TWIF**	TWI Interrupt flag 0: Cleared to zero by software 1: The Interrupt flag is set to 1 by hardware under the following conditions ①First frame address matched ②Successfully received or transmitted 8-bit data ③Restart ④Slave received a Stop Signal
4	**GCA**	General Address Response Flag 0: Does not respond to the General Address 1: When GC is set to 1 and the General Address matches, this bit is set by hardware and automatically cleared
3	**AA**	Receive Enable bit 0: Receiving messages transmitted by the Host is not allowed 1: Receiving messages transmitted by the Host is allowed
2 ~ 0	**STATE[2:0]**	State machine status flag bits 000: Slave is in the Idle State, waiting for TWEN to be set to 1 and for a TWI start signal to be detected. After the Slave receives a stop condition, it transitions to this state 001: Slave receiving first frame address and read/write bit (bit 8: 1=read, 0=write). Transitions to this state after detecting a start condition. 010: Slave receiving data state 011: Slave sending data state 100: During Slave sending data state, transitions to this state when the Host returns UACK (acknowledge bit is high), waiting for a restart signal or stop signal. 101: Slave waiting for restart or stop condition after clearing AA bit during data sending
5	**-**	Reserved

SSCON1 (9EH) TWI Address Register (R/W)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	TWA[6:0]							GC
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7 ~ 1	**TWA[6:0]**	TWI Address Register
0	**GC**	TWI General Address Enable 0: Do not respond to the General Address 1: Respond to the General Address

SSDAT (9FH) TWI Data Buffer Register (R/W)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	TWDAT[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7 ~ 0	**TWDAT[7:0]**	TWI Data Buffer Register

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17.2.1 Signal description

17.2.1.1 TWI clock signal line (SCL)

This clock signal is generated by the master and connected to all slaves. One byte of data is transmitted every 9 clock cycles. The first 8 cycles are used to transmit data, and the last clock cycle is used as the receiver's acknowledge clock.

17.2.1.2 TWI data signal line (SDA)

SDA is a bidirectional signal line that should be high when idle, pulled high by a pull-up resistor on the SDA line.

17.2.2 Operating mode

The SC92R425B supports only Slave mode for TWI Communication:

- **Mode enabled**

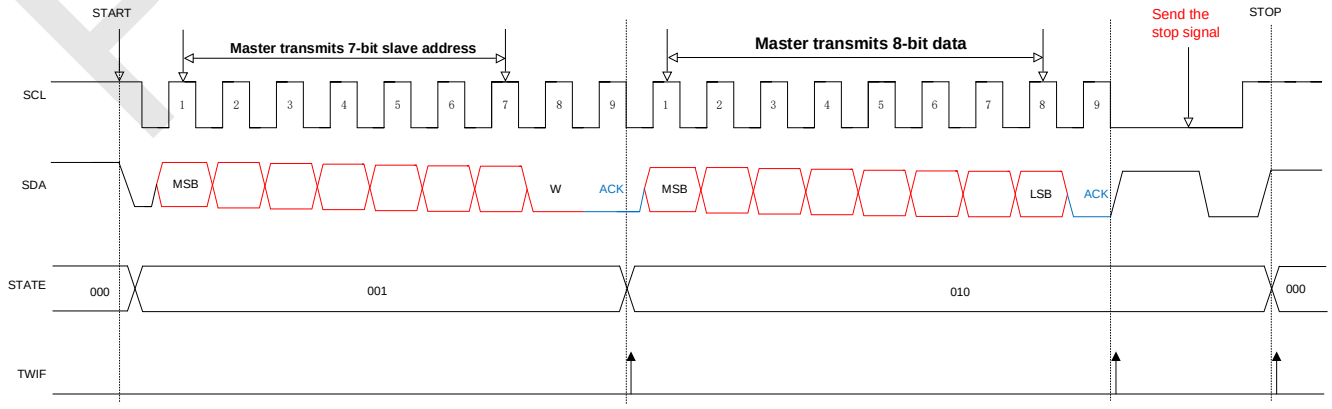
When the TWI enable flag is set (TWEN = 1) and a Start signal from the master is received, the mode starts.

The Slave transitions from idle mode (STATE[2:0] = 000) to the Receive First-Frame Address state (STATE[2:0] = 001), where it waits for the master's first-frame data. The first-frame data is sent by the Host and includes a 7-bit address and a 1-bit Read/Write Bit. All Slaves on the TWI Bus receive the Host's first-frame data. After transmitting the first-frame data, the Host releases the SDA signal line. If the address sent by the Host matches the value in a Slave's own Address Register, that Slave is selected. The selected Slave checks the 8th bit on the Bus, namely the Read/Write Bit (=1, read command; =0, write command), then takes control of the SDA signal line and sends the Host a Low-level Acknowledge signal during the 9th Clock Cycle of SCL, after which it releases the Bus. After a Slave is selected, it enters a different state depending on the Read/Write Bit:

- **Non-General-Purpose Address Response, Slave Receive Mode**

If the Read/Write Bit received in the first frame is write (0), the Slave enters the Slave Receive state (STATE[2:0] = 010) and waits to receive Data sent by the Host. After transmitting every 8 bits, the Host must release the Bus and wait for the Slave's Acknowledge signal during the 9th Period.

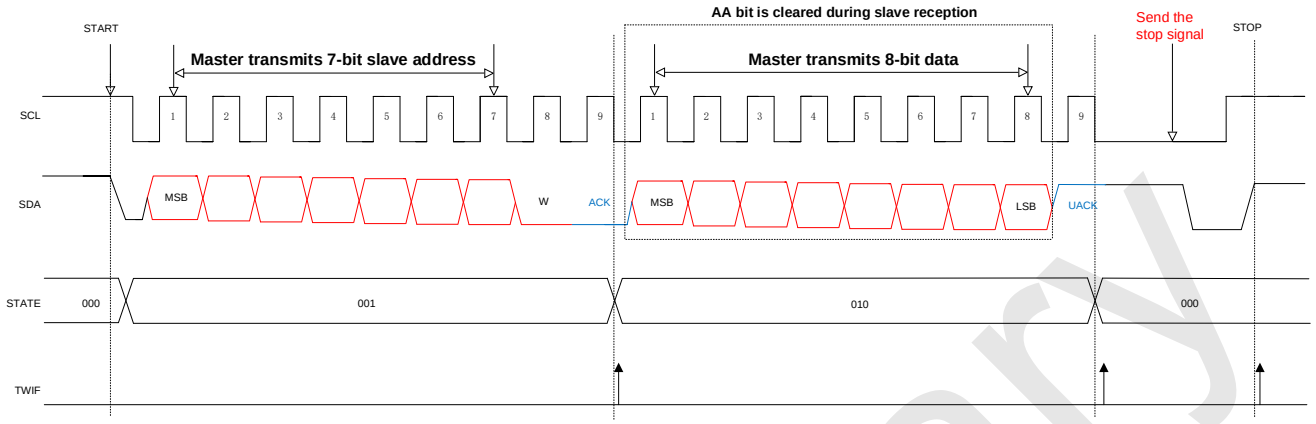
1. If the Slave's Acknowledge signal is Low level, the Host can proceed with Communication in one of the following three ways:
   1) Continue transmitting Data
   2) Transmit a Start signal again; the Slave then re-enters the Receive First-Frame Address state (STATE[2:0] = 001)
   3) Transmit a Stop Signal to indicate the end of this transmission; the Slave returns to the Idle State and waits for the Host's next Start signal.



2. If the Slave acknowledges with a high level (during reception, the AA value in the Slave Register is rewritten to 0), this indicates that after the current Byte is transferred, the Slave will actively end the

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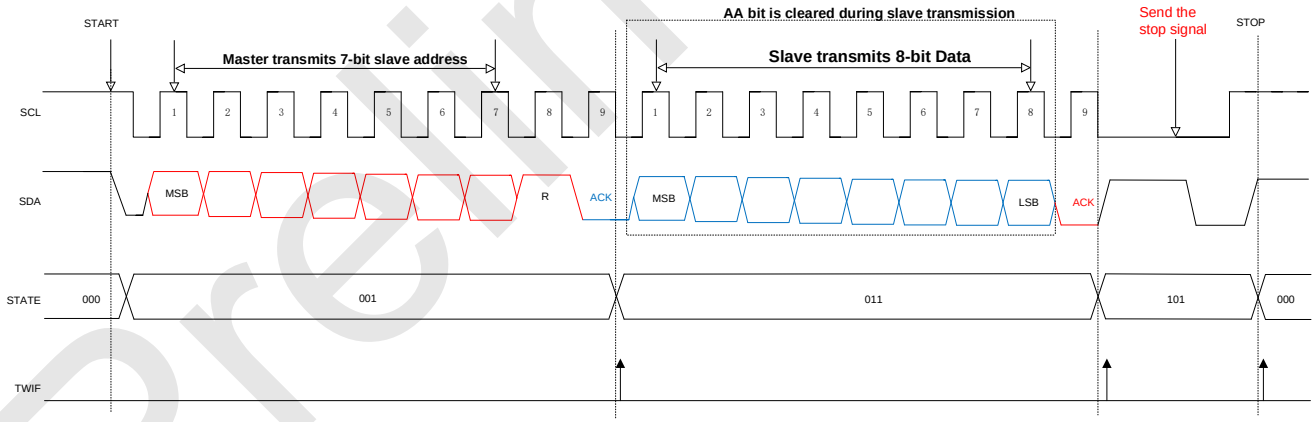
current transfer and return to the Idle State (STATE[2:0] = 000), without receiving any more Data transmitted by the Host.



- **Non-General-Purpose Address Response, Slave Transmit Mode**

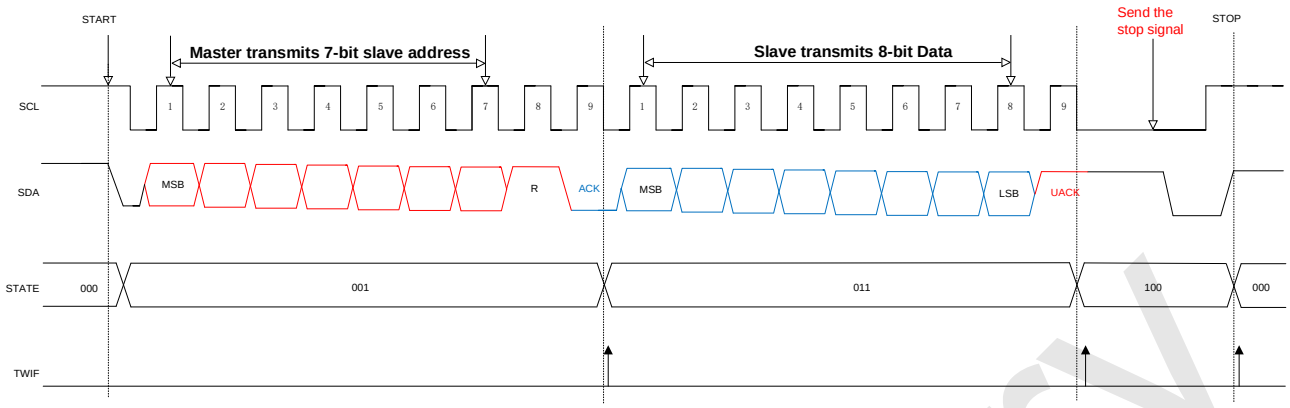
If the Read/Write Bit received in the first frame is Read (1), the Slave will take control of the Bus and transmit Data to the Host. After transmitting each 8-bit Data unit, the Slave releases the Bus and waits for the Host's Acknowledge:

1. If the Host acknowledges with a low level, the Slave continues transmitting Data. During transmission, if the AA value in the Slave Register is rewritten to 0, the Slave will actively end the transfer after completing the current Byte and release the Bus, waiting for the Host's Stop Signal or Restart signal (STATE[2:0] = 101).



2. If the Host acknowledges with a high level, the Slave enters STATE[2:0] = 100 and waits for the Host's Stop Signal or Restart signal.

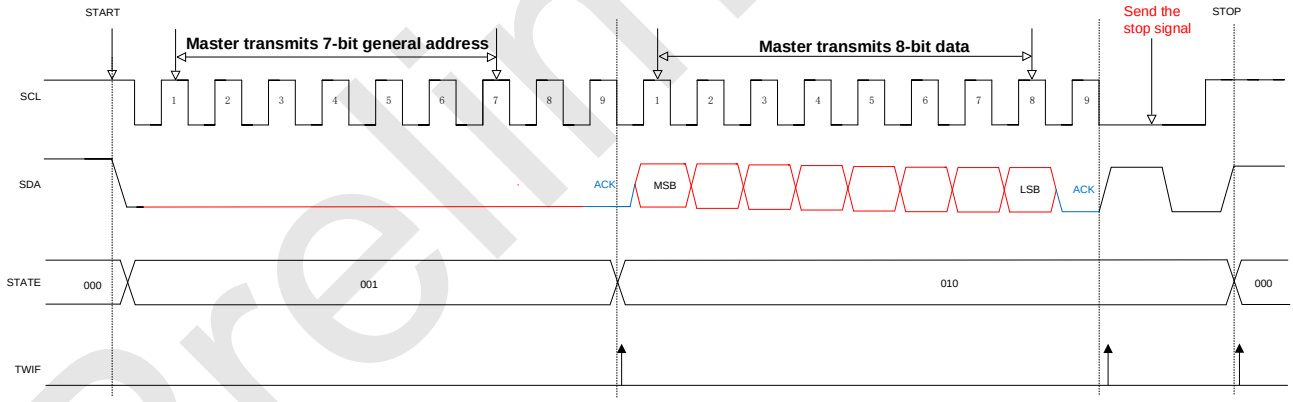
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- **General Address Response**

When GC=1, the General Address is enabled. The Slave enters the Receive First-Frame Address state (STATE[2:0] = 001). If the address bit data in the received First-Frame Data is 0x00, all Slaves respond to the Host. The Read/Write Bit sent by the Host must be Write (0). After receiving it, all Slaves enter the Receive Data state (STATE[2:0] = 010). After transmitting every 8 bits of data, the Host releases the SDA line once and reads its status:

1. If a Slave acknowledges, the Host can communicate in any of the following three ways:
   1) Continue transmitting Data
   2) Restart
   3) Transmit the Stop Signal to end this communication.



2. If no Slave responds, SDA remains in the Idle State.

Note: When using a General Address in a single-master multi-slave setup, the master's Read/Write Bit cannot be set to read (1). Otherwise, all other devices on the Bus except the device transmitting Data will respond.

17.2.3 Operating procedure

The operating procedure for TWI mode in the Three-in-One Serial Port is as follows:

1. Configure SSMOD[1:0] to select TWI mode
2. Configure the SSCON0 TWI Control Register
3. Configure the SSCON1 TWI Address Register
4. If the Slave receives data, wait for the TWIF Interrupt flag in SSCON0 to be set to 1. The Interrupt flag is set to 1 each time the Slave receives 8 bits of data, and must be cleared manually

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5. If the Slave transmits data, write the data to be transmitted to TWDAT, and TWI will transmit it automatically. The TWIF Interrupt flag is set to 1 after every 8 bits are transmitted.

17.3 UART1

SSMOD[1:0] = 11, the One-of-three serial interface SSI is configured as a UART interface.

SSCON0 (9DH) Serial Port 1 Control Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	SM0	-	SM2	REN	TB8	RB8	TI	RI
Read/Write	R/W	-	R/W	R/W	R/W	R/W	R/ W1 to clear	R/ W1 to clear
Power-On Initial Value	0	x	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7	**SM0**	Serial Communication Mode Control Bit 0: Mode 1, 10-bit Full-Duplex Asynchronous Communication, consisting of 1 Start Bit, 8 Data Bits, and 1 Stop Bit; variable Communication Baud Rate 1: Mode 3, 11-bit Full-Duplex Asynchronous Communication, consisting of 1 Start Bit, 8 Data Bits, 1 Programmable 9th Bit, and 1 Stop Bit; variable Communication Baud Rate
5	**SM2**	Serial Communication Mode Control Bit 2; this Control Bit is valid only in Mode 3 0: RI is set and an Interrupt Request is generated each time a complete Data Frame is received 1: When a complete Data Frame is received, RI is set and an Interrupt Request is generated only when RB8=1.
4	**REN**	Receive Enable Control Bit 0: Data reception is disabled 1: Data reception is enabled.
3	**TB8**	Valid only in Mode 3; this is the 9th Bit of Transmitted Data
2	**RB8**	Valid only in Mode 3; this is the 9th Bit of Received Data
1	**TI**	Transmit Interrupt flag This bit is set to 1 by hardware upon Transmission complete and must be cleared by writing 1 in software
0	**RI**	Receive Interrupt flag This bit is set to 1 by hardware upon Receive complete and must be cleared by writing 1 in software
6	**-**	Reserved

SSCON1 (9EH) Serial Port 1 Baud Rate Control Register Low-order bit (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	BAUDL [7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

SSCON2 (95H) Serial Port 1 Baud Rate Control Register Most Significant Bit (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	BAUDH [7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

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Bit Number	7	6	5	4	3	2	1	0
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7 ~ 0	**BAUD [15:0]**	**Serial Port Baud Rate Control** $\text{BaudRate} = \frac{\text{fsys}}{\text{BAUD1H, BAUD1L}}$ **Note: [BAUD1H,BAUD1L] must be greater than 0x0010**

SSDAT (9FH)Serial Port Data Buffer Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	SBUF[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7 ~ 0	**SBUF[7:0]**	**Serial Port Data Buffer Register** SBUF contains two registers: a Transmit Shift Register and a Receive Latch. Data written to SBUF is sent to the Transmit Shift Register and starts the transmission process; reading SBUF returns the contents of the Receive Latch.

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18 ADC

The SC92R425B integrates 27 channels of 12-bit high-precision successive-approximation ADC. The 26 external ADC channels are multiplexed with other functions of the IO pins; one internal channel can be connected to 1/4 VDD and used with the internal 1.024 V, 2.4 V, or 2.048 V Reference voltage to measure VVDD.

The SC92R425B ADC offers four Reference voltage options:

1. The VDD Pin (directly using the internal VDD)
2. A precise 1.024 V Reference voltage output by the Internal Regulator.
3. A precise 2.4 V Reference voltage output by the Internal Regulator.
4. A precise 2.048 V Reference voltage output by the Internal Regulator.

18.1 ADC-related registers

ADCCON (ADH) ADC Control Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	ADCEN	ADCS	ADCIF	ADCIS[4:0]				
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	n

Bit Number	Bit Symbol	Description
7	**ADCEN**	ADC power supply enable 0: Turn off the ADC module power supply 1: Turn on the ADC module power supply
6	**ADCS**	ADC start trigger control (ADC Start) Write "1" to this bit to start one ADC conversion; this bit serves only as the ADC Conversion trigger signal. Only writing 1 to this bit is valid. **Note: After writing "1" to ADCS, do not write to the ADCCON Register until the Interrupt flag ADCIF is set**
5	**ADCIF**	ADC Interrupt Request Flag (ADC Interrupt Flag) 0: Conversion is not complete 1: ADC conversion complete. Must be cleared by user software ADC Interrupt Request Flag ADCIF: This bit also serves as the interrupt request flag for the ADC interrupt. If the user enables the ADC interrupt, this bit must be cleared by software after the ADC interrupt occurs.
4 ~ 0	**ADCIS[4:0]**	ADC Input Channel Selection (ADC Input Selector) 00000: Select AIN0 as the ADC input 00001: Select AIN1 as the ADC input 00010: Select AIN2 as the ADC input 00011: Select AIN3 as the ADC input 00100: Select AIN4 as the ADC input 00101: Select AIN5 as the ADC input 00110: Select AIN6 as the ADC input 00111: Select AIN7 as the ADC input 01000: Select AIN8 as the ADC input 01001: Select AIN9 as the ADC input 01010: Select AIN10 as the ADC input 01011: Select AIN11 as the ADC input 01100: Select AIN12 as the ADC input 01101: Select AIN13 as the ADC input 01110: Select AIN14 as the ADC input 01111: Select AIN15 as the ADC input 10000: Select AIN16 as the ADC input

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Bit Number	Bit Symbol	Description
		10001: Select AIN17 as the ADC input 10010: Select AIN18 as the ADC input 10011: Select AIN19 as the ADC input 10100: Select AIN20 as the ADC input 10101: Select AIN21 as the ADC input 10110: Select AIN22 as the ADC input 10111: Select AIN23 as the ADC input 11000: Select AIN24 as the ADC input 11001: Select AIN25 as the ADC input 11010 to 11110: Reserved 11111: ADC input is 1/4 V_{DD} ; can be used to measure the supply voltage

ADCCFG2 (AAH) ADC Configuration Register 2 (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	AINX[1:0]		-	LOWSP[2:0]			ADCCK[1:0]	
Read/Write	R/W	R/W	-	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	x	0	0	0	0	0

Bit Number	Bit Symbol	Description
4 ~ 2	**LOWSP[2:0]**	**SC92R425B, ADC sampling time selection:** 000: ADC sampling time is approximately 20 ADC Clock Cycles 001: ADC Sampling Time is approximately 50 ADC Clock Cycles 010: ADC Sampling Time is approximately 20 ADC Clock Cycles 011: ADC Sampling Time is approximately 50 ADC Clock Cycles Description: 1. LOWSP[2:0] controls the number of ADC Sampling Clock Cycles, and ADCCK[1:0] controls the ADC Sampling Clock Frequency 2. The ADC requires approximately 20 or 50 ADC Sampling Clock Cycles plus approximately 16 ADC Conversion Clock Cycles to complete the entire process from sampling to conversion. Therefore, in actual use, the total time from ADC sampling to completion of conversion is calculated as follows: ● LOWSP=000 or 010: $T_{ADC1}=20/f_{SYS}+16/f_{ADC}$ ● LOWSP=001 or 011: $T_{ADC2}=50/f_{SYS}+16/f_{ADC}$
1 ~ 0	**ADCCK[1:0]**	ADC Sampling Clock Frequency Selection (ADC Sampling Clocks Selector) 00: Set the ADC Clock Frequency f_{ADC} to $f_{SYS}/16$ 01: Set the ADC Clock Frequency f_{ADC} to f_{SYS} 12 10: Set the ADC Clock Frequency f_{ADC} to $f_{SYS}/6$ 11: Set the ADC Clock Frequency f_{ADC} to $f_{SYS}/4$
7 ~ 6	**AINX[1:0]**	**ADC Channel Register Pointer** For details, see AINX[1:0] ADC Channel Register Pointer
5	**-**	Reserved

AINX[1:0] ADC Channel Register Pointer:

Note:

1. **The user must set AINX[1:0] before reading from or writing to ADCCFG0. AINX automatically increments by 1 (cycling from 0 to 3) each time the ADCCFG0 Register is read or written.**
2. **When the Chip core executes ORL and ANL instructions, it performs a read followed by a write; therefore, AINX increments by 2 each time an ORL or ANL instruction is executed.**

ADCCFG0 (ABH) ADC Configuration Register 0 (R/W)

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Symbol	Address	Description	7	6	5	4	3	2	1	0
ADC_CHN	ABH	ADC Channel Selection Register	EAINx[7:0]							

ADCCFG0 is actually the address of four ADC channel registers, ADC_CHNn (n=0 to 3); the ADC channel register currently being accessed is determined by AINX[1:0]:

Symbol	Address @ ABH	Description	7	6	5	4	3	2	1	0
ADC_CHN3	AINX [1:0] = 11	ADC Channel Selection Register 3	-	-	-	-	-	-	EAIN25	EAIN24
ADC_CHN2	AINX[1:0] = 10	ADC Channel Selection Register 2	EAIN23	EAIN22	EAIN21	EAIN20	EAIN19	EAIN18	EAIN17	EAIN16
ADC_CHN1	AINX [1:0] = 01	ADC Channel Selection Register 1	EAIN15	EAIN14	EAIN13	EAIN12	EAIN11	EAIN10	EAIN9	EAIN8
ADC_CHN0	AINX [1:0] = 00	ADC Channel Selection Register 0	EAIN7	EAIN6	EAIN5	EAIN4	EAIN3	EAIN2	EAIN1	EAIN0

ADC_CHN0 (ABH) ADC Channel Register 0 (R/W)

@ AINX [1:0] = 00

Bit Number	7	6	5	4	3	2	1	0
Symbol	EAIN7	EAIN6	EAIN5	EAIN4	EAIN3	EAIN2	EAIN1	EAIN0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

ADC_CHN1 (ABH) ADC Channel Register 1 (R/W)

@ AINX [1:0] = 01

Bit Number	7	6	5	4	3	2	1	0
Symbol	EAIN15	EAIN14	EAIN13	EAIN12	EAIN11	EAIN10	EAIN9	EAIN8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

ADC_CHN2 (ABH) ADC Channel Register 2 (R/W)

@ AINX [1:0] = 10

Bit Number	7	6	5	4	3	2	1	0
Symbol	EAIN23	EAIN22	EAIN21	EAIN20	EAIN19	EAIN18	EAIN17	EAIN16
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

ADC_CHN3 (ABH) ADC Channel Register 3 (R/W)

@ AINX [1:0] = 11

Bit Number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	EAIN25	EAIN24
Read/Write	-	-	-	-	-	-	R/W	R/W
Power-On	x	x	x	x	x	x	0	0

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Bit Number	7	6	5	4	3	2	1	0
Initial Value								

Bit Number	Bit Symbol	Description
7 ~ 0	**EAINx (x=0 to 25)**	**ADC Port Configuration Register** 0: The port corresponding to AINx cannot be used as an ADC input channel 1: The corresponding port for AINx can be used as an ADC input channel. When ADCIS[4:0] selects AINx as the ADC input channel, the Pull-up resistor on the corresponding AINx port is automatically removed.

OP_CTM1 (C2H@FFH)Customer Option Register 1 (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	VREFS[1:0]		OP_BL	DISJTG	IAPS[1:0]		LDSIZE[1:0]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R	
Power-On Initial Value	n	n	n	n	n	n	n	n

Bit Number	Bit Symbol	Description
7 ~ 6	**VREFS[1:0]**	**Reference Voltage Selection (initial value loaded from Code Option; user-configurable)** 00: Set the ADC V_{REF} to V_{DD} 01: Set the ADC V_{REF} to the precise internal 1.024 V 10: Set the ADC V_{REF} to the precise internal 2.4 V 11: Set the ADC V_{REF} to the accurate internal 2.048 V

ADCVL (AEH) ADC Conversion Value Register (Low-order bit) (R)

Bit Number	7	6	5	4	3	2	1	0
Symbol	ADCV[3:0]				-	-	-	-
Read/Write	R	R	R	R	-	-	-	-
Power-On Initial Value	1	1	1	1	x	x	x	x

ADCVH (AFH) ADC Conversion Value Register (Most Significant Bit) (R)

Bit Number	7	6	5	4	3	2	1	0
Symbol	ADCV[11:4]							
Read/Write	R	R	R	R	R	R	R	R
Power-On Initial Value	1	1	1	1	1	1	1	1

Bit Number	Bit Symbol	Description
11 ~ 4	**ADCV[11:4]**	The High 8 Bits of the ADC Conversion Value
3 ~ 0	**ADCV[3:0]**	The Low 4 Bits of the ADC Conversion Value

IE (A8H) Interrupt Enable Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	EA	EADC	ET2	EUART	ET1	EINT1	ET0	EINT0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

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Bit Number	Bit Symbol	Description
6	**EADC**	ADC interrupt enable control 0: Disable ADCIF interrupt generation 1: Enable ADCIF interrupt generation

IP (B8H) Interrupt Priority Control Register (R/W)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	-	IPADC	IPT2	IPUART	IPT1	IPINT1	IPT0	IPINT0
Read/Write	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	x	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
6	**IPADC**	ADC interrupt priority selection 0: Set the ADC interrupt priority to low 1: Set the ADC interrupt priority to high

18.2 ADC conversion steps

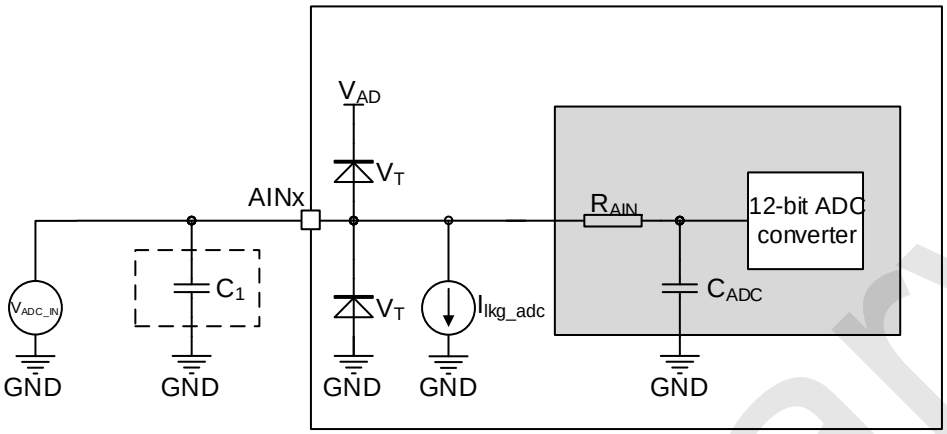
The operating procedure for performing an ADC conversion is as follows:

1. Set the ADC input Pin; (Select AINx as the ADC input using the ADC Channel Register Pointer AINX[1:0] in conjunction with the ADCCFG0 Register; the ADC Pin is usually fixed in advance)
2. Set the ADC reference voltage Vref and the Frequency used for ADC Conversion
3. Use LOWSP[2:0] and ADCCK[1:0] to set the fast or slow mode and the corresponding Sampling Time
4. Enable the ADC Module Power Supply
5. Select the ADC Input Channel (set the ADCIS bit to select the ADC Input Channel)
6. Set ADCS to start conversion
7. Wait for ADCIF = 1. If the ADC interrupt is enabled, an ADC interrupt will be generated, and the user must clear the ADCIF flag in software
8. Read the 12-bit conversion result from ADCVH and ADCVL (high byte first, then low byte). One conversion is complete
9. If the input channel remains unchanged, repeat steps 6-8 to perform the next conversion.

Note: Before setting IE[6] (EADC), users are advised to clear ADCIF in software first. ADCIF should also be cleared when the ADC Interrupt Service Routine finishes executing to prevent ADC interrupts from being generated continuously.

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18.3 ADC connection circuit diagram



Description:

- C1 is an external 0.01μF capacitor; users are advised to add this capacitor to improve ADC performance
- For ADC electrical specifications, see Chapter 23.7 ADC Electrical Characteristics.

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19 High-sensitivity Touch Circuit

The SC92R425B has a built-in 24-channel high-sensitivity touch circuit with the following features:

1. High-sensitivity mode supports touch applications requiring high sensitivity, such as touchless key touch and proximity sensing
2. Supports 24 touch keys and derivative functions, with channels configurable for parallel scanning
3. Internal or external CMOD can be selected. When external CMOD is selected, connect a 103 capacitor from the CMOD Pin to ground
4. Software library support for highly flexible development with low development complexity
5. Supports automated debugging software for intelligent development
6. The touch module can enter low-power mode while the MCU is in STOP mode

Note: When selecting an external CMOD capacitor, be sure to connect an external capacitor as the TK charging capacitor; otherwise, the touch function will not work properly

19.1 Touch circuit power consumption modes

The SC92R425B allows Touch scanning to be enabled in STOP Mode, reducing the MCU's overall power consumption to meet the needs of Touch applications requiring low power.

The Touch circuit of the SC92R425B can be understood as having two power consumption modes:

1. Normal operation mode
2. Low-power operation mode

The two power consumption modes are defined as follows:

Description	Normal operation mode	Low-power operation mode
CPU	RUN (Normal mode)	Stop (STOP Mode)
Touch circuit	RUN	RUN

Note: Users can quickly and easily implement the required Touch functions by using the Touch key library provided by SinOne, which can be downloaded from the SinOne website.

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20 Water-level detection module

The SC92R425B has a built-in Water-Level Detection Module that supports up to 8 water-level detection levels. SinOne provides a Water-Level Detection library for users to call, reducing the development difficulty of the water-level detection section. For detailed instructions, please refer to:

SC92R425B_WL_TK_Lib User Manual.

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21 CRC module

The SC92R425B has one built-in Hardware CRC module. During CRC calculation, the CPU holds the Program Counter; the Program Counter resumes executing subsequent Instructions only after the CRC calculation is complete. The module has two calculation modes.

Hardware CRC Mode 1: Perform CRC calculation on specified Data

Write the Data to be processed by CRC calculation to the CRC Data Register CRCREG. To Read the CRC calculation result, Read it from CRCDRn (n = 0 to 3).

Calculating the CRC for a single byte requires 8 System Clocks, i.e., 0.8 μs@10 MHz. 0.8μs@10 MHz

Hardware CRC Mode 2: Perform CRC calculation on APROM

Can be used to generate the 32-bit CRC value of APROM (i.e., 16 Kbytes Flash ROM) in real time. Comparing this value with the theoretical value can monitor whether the contents of the program area are correct. The theoretical CRC value does not need to be calculated by the user. The programming software automatically calculates it based on the loaded code and Code Area settings, then writes the 4-byte CRC32 result to the CRC result storage area via the Programmer during programming. For details, see the Programming Tool User Manual.

Calculating the CRC for 16 Kbytes of APROM takes approximately 13 ms @ 10 MHz.

CRC algorithm name	CRC-32/MPEG-2
Polynomial Formula	$x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^8+x^7+x^5+x^4+x^2+x+1$
Data Width	32bit
Initial value	0xFFFFFFFF
Final XOR Value	0x00000000
Input Data Reflection	false
Output Data Reflection	false
LSB/MSB	MSB

CRC usage notes:

1. **Data written to and read from CRCDRn are not the same.**
2. **The CRC value calculated by the hardware is the 32-bit CRC verification value for the entire program area (note that this does not include the IAP Area!). If the address unit contains a residual value from the user's previous operation, the CRC value will not match the theoretical value. Therefore, users are advised to erase the entire Flash ROM before programming code to ensure that the CRC value matches the theoretical value.**
3. **The hardware CRC calculation range does not include the IAP Area.**
4. **If users need to perform a CRC calculation. Please refer to the "SC92R425B CRC Operation Library Package".**

21.1 Registers related to CRC verification

OPERCON (EFH) Operation Control Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	OPERS	MD	-	-	-	-	CRCRST	CRCSTA
Read/Write	R/W	R/W	-	-	-	-	R/W	R/W
Power-On Initial Value	0	0	x	x	x	x	0	0

Bit Number	Bit Symbol	Description
1	CRCRST	Reset CRCDR Register (Q31 to Q0) Write "1" to this bit to reset CRCDR to all 1 s
0	CRCSTA	Hardware CRC Calculation Start Bit

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Bit Number	Bit Symbol	Description
		Write "1" to this bit to start a Check sum calculation. Only writing 1 to this bit is valid.

Read and write operations on the CRC data registers CRCDRn (n = 0 to 3) are controlled by the CRCINX and CRCREG registers. The specific location of each CRCDRn is determined by CRCINX, as shown in the table below:

Symbol	Address	Description	7	6	5	4	3	2	1	0	Power-On Initial Value
CRCINX	FCH	CRC Pointer	CRCINX[7:0]								00000000b
CRCREG	FDH	CRC Register	CRCREG[7:0]								nnnnnnnnb

Symbol	Address	Description	7	6	5	4	3	2	1	0
CRCDR3	03H at FDH	CRC Data Register 3	Q31	Q30	Q29	Q28	Q27	Q26	Q25	Q24
CRCDR2	02H at FDH	CRC Data Register 2	Q23	Q22	Q21	Q20	Q19	Q18	Q17	Q16
CRCDR1	01H at FDH	CRC Data Register 1	Q15	Q14	Q13	Q12	Q11	Q10	Q9	Q8
CRCDR0	00H at FDH	CRC Data Register 0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0

Bit descriptions for CRCDRn (n = 0~3) are as follows:

Bit Number	Sign bit	Description
31 ~ 0	Qx (x = 0 to 31)	Hardware CRC Mode 1: Perform CRC calculation on specified data: 1. First, write CRCRST to reset CRCDR to all 1 s 2. When CRCREG is written, the hardware automatically calculates the CRC result and continues to store it in CRCDR 3. Read the CRC calculation result immediately when needed Hardware CRC Mode 2: Perform CRC calculation on APROM: 1. Started by CRCSTA; the CPU automatically enters IDLE 2. Automatically reset CRCDR to all 1 s: 3. **The hardware CRC calculation range does not include the IAP Area.** The CRC calculation range is divided into four cases according to the value of IAPS[1:0]: 1) IAPS[1:0]=00 (the last 0K of Flash ROM is available for IAP): 0000H to before the last 0K 2) IAPS[1:0]=01 (the last 0.5K of Flash ROM is available for IAP): 0000H to before the last 0.5K 3) IAPS[1:0]=10 (the last 1K of Flash ROM is available for IAP): 0000H to before the last 1K 4) IAPS[1:0]=11 (all of Flash ROM is available for IAP): all Flash ROM 4. After completion, the CPU automatically exits IDLE, and the CRC calculation result can then be read Note: The data written and the data read out are not the same.

When operating CRC-related SFRs, the CRCINX Register stores the Address of the corresponding CRCREG Register, and the CRCREG Register stores the corresponding value. Before reading CRCREG, set CRCINX. After each read, CRCINX automatically increments by 1 (cycles from 0 to 3).

Note: Do not write any value other than a CRC Register address to the CRCINX Register! Otherwise, the system may operate abnormally!

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22 LED Drive

22.1 Features

- 16 LED drive pins in total: LED0-LED15
- The source drive capability of all LED pins is controlled in 16 levels
- LED0 to LED15, 16 channels in total, each providing 150 mA@0.8 V High Sink Current
- The IC System Clock (f_{SYS}) is used as the LED clock source
- After one LED scan frame is completed, the corresponding LED driver flag bit AUIF is set to 1
- The SEG output period width matches the COM width during auto-scanning
- LED dead time design requirement: between 10 μs and 3 μs
- LED supports two modes
- Bidirectional drive mode:
  - LED0 to LED11 support bidirectional drive mode and can jointly drive up to 11 × 12 Pixels
  - 12 scan modes available, from "11 × 12" to "1 × 1"
  - Common Port LED0, with 4 selectable Scan Times: 0.5T, 1T, 1.5T, and 2T
- Normal mode:
  - 8 COM and 12 SEG pins, with four COM pins multiplexed with SEG
  - Can be configured for 8 × 8, 6 × 10, 5 × 11, or 4 × 12 segment LED drive
  - Scan cycle is fixed at 1T

22.2 LED-related pins

The following table adds the COM and SEG information for LED normal mode to the pin list:

28PIN	20PIN	16PIN	8PIN	IO	LED push-pull	LED normal
9	7	7	-	P1.4	LED0	LED0 (C7)
10	8	8	-	P1.5	LED1	LED1 (C6)
11	-	-	-	P1.6	LED2	LED2 (C5)
12	-	-	-	P1.7	LED3	LED3 (C4)
13	9	-	-	P2.7	LED4	LED4 (C3/S0)
14	10	9	-	P2.6	LED5	LED5 (C2/S1)
15	11	10	5	P2.5	LED6	LED6 (C1/S2)
16	12	11	6	P2.4	LED7	LED7 (C0/S3)
17	-	-	-	P2.3	LED8	LED8 (S4)
18	-	-	-	P2.2	LED9	LED9 (S5)
19	13	12	7	P2.1	LED10	LED10 (S6)
20	14	13	-	P2.0	LED11	LED11 (S7)
21	-	-	-	P0.7		LED12 (S8)
22	-	-	-	P0.6		LED13 (S9)
23	15	14	-	P0.5		LED14 (S10)
24	16	-	-	P0.4		LED15 (S11)

Note: Only LED0 to LED11 support bidirectional drive mode.

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22.3 LED display driver registers

Symbol	Address	Description	7	6	5	4	3	2	1	0	Power-On Initial Value
LEDVO1	93H	LED Display Driver Output Register 1	LED15VO	LED14VO	LED13VO	LED12VO	LED11VO	LED10VO	LED9VO	LED8VO	00000000b
DDRCON	96H	Display driver control register	DDRON	DMOD	DUTY[1:0]		DRIV[3:0]				00001111b
SCANCON	97H	Display driver scan configuration register	AUIF	CMEN	LEDXT[1:0]		LTSEL[1:0]		LEDCK[1:0]		00010000b
LEDVO0	9CH	LED Display Driver Output Register 0	LED7VO	LED6VO	LED5VO	LED4VO	LED3VO	LED2VO	LED1VO	LED0VO	00000000b

The registers are described as follows:

22.3.1 LEDVO0 (9CH)LED display driver output register 0 (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	LED7VO	LED6VO	LED5VO	LED4VO	LED3VO	LED2VO	LED1VO	LED0VO
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

22.3.2 LEDVO1 (93H)LED display driver output register 1 (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	LED15VO	LED14VO	LED13VO	LED12VO	LED11VO	LED10VO	LED9VO	LED8VO
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7 ~ 0	**LEDnVO n=0 to 15**	**Enable LEDn port display driver output** 0: Disable the display driver output function of the LEDn port 1: Enable the display driver output function of the LEDn port **Note: In bidirectional drive mode, the number of scans depends on the number of LEDn functions selected.** For example: ● Bidirectional drive mode: The user enables 5 LED drive ports; the actual Scan Duty is 1/5 ● Normal mode: The user enables 3 COMs; the actual Scan Duty is 1/3

22.3.3 DDRCON (96H) display driver control register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	DDRON	DMOD	DUTY[1:0]		DRIV[3:0]			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	1	1	1	1

Bit Number	Bit Symbol	Description
7	**DDRON**	**LED Display Driver enable control** 0: Display driver scanning off 1: Display driver scanning on; Constant-current source enabled

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Bit Number	Bit Symbol	Description
		simultaneously
6	**DMOD**	**LED Display Driver mode** 0: Normal mode LED; Display RAM (400H to 40FH) used for Normal mode scanning 1: Bidirectional drive mode LED; Display RAM (400H to 417H) used for Forward/Reverse Scanning
5 ~ 4	**DUTY[1:0]**	**Normal mode LED display Duty cycle control** 00: S4 to S11 are segments, C0 to C7 are commons 01: S2 to S11 are segments, C2 to C7 are commons 10: S1 to S11 are segments, C3 to C7 are commons 11: S0 to S11 are segments, and C4 to C7 are commons
3 ~ 0	**DRIV[3:0]**	**Constant-current source output current selection bits** The higher the DRIV[3:0] setting, the higher the current; the lower the DRIV[3:0] setting, the lower the current Power-On Initial Value is 1111: 20 mA The constant-current source setting applies to all enabled LED ports

Serial Number	DRIV[3:0]	Parameter
0	0000	Brightness Level 1
1	0001	Brightness Level 2
2	0010	Brightness Level 3
3	0011	Brightness Level 4
4	0100	Brightness Level 5
5	0101	Brightness Level 6
6	0110	Brightness Level 7
7	0111	Brightness Level 8
8	1000	Brightness Level 9
9	1001	Brightness Level 10
10	1010	Brightness Level 11
11	1011	Brightness Level 12
12	1100	Brightness Level 13
13	1101	Brightness Level 14
14	1110	Brightness Level 15
15	1111	Brightness Level 16

22.3.4 SCANCON (97H) Display driver scan configuration register (R/W)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	AUIF	CMEN	LEDXT[1:0]		LTSEL[1:0]		LEDCK[1:0]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	1	0	0	0	0

Bit Number	Bit Symbol	Description
7	**AUIF**	**Frame scan completion flag** 0: Scan not complete 1: Frame scan complete; set to 1 by hardware, cleared to 0 by writing 1 in software
6	**CMEN**	**IO port constant-current output mode enable bit** 0: IO constant-current output mode disabled 1: IO constant-current output mode enabled; IO ports selected by

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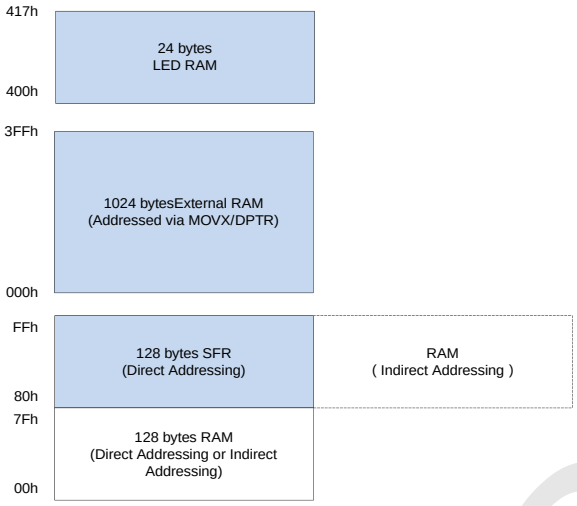
<table>
<tr><th>Bit Number</th><th>Bit Symbol</th><th>Description</th></tr>
<tr><td></td><td></td><td>LEDnVO output constant current</td></tr>
<tr><td>5 ~ 4</td><td>LEDXT[1:0]</td><td>LED-specific scan port scan time setting bits
00: 0.5T
01: 1T-power-on default
10: 1.5T
11: 2T
Description:
1. The LED-specific scan port is set by LTSEL[1:0]
2. At power-on, the display mode defaults to 11 segments × 12 digits, and the scan time defaults to "1T"

"1T" is approximately the length of one LED Clock (as set by LEDCK[1:0]).</td></tr>
<tr><td>3 ~ 2</td><td>LTSEL[1:0]</td><td>LED-specific scan port selection bits:
00: LED0
01: LED1
10: LED8
11: LED9
For the selected LEDn (n=0, 1, 8, 9), the scan time varies according to the LEDXT[1:0] setting.</td></tr>
<tr><td>1 ~ 0</td><td>LEDCK[1:0]</td><td>LED module Clock frequency division:
00: f_{SYS} / 8192
01: f_{SYS} / 16384
10: f_{SYS} / 32768
11: f_{SYS} / 65536
Note: To ensure good display performance, set the LED Dead Time as close as possible to 10 μs to 3 μs.
The following three cases are recommended:
（1） LEDCK=00, System Clock Frequency 5 MHz, dead time 6 μs
（2） LEDCK=00, System Clock Frequency 10 MHz, dead time 3 μs
（3） LEDCK=01, System Clock Frequency 10 MHz, dead time 6 μs.
LED Dead Time is related to LEDCK[1:0] and System Clock Frequency f_{SYS}, as shown in the following table:
<table>
<tr><th>LEDCK[1:0]</th><th>f_{SYS}=5MHz</th><th>f_{SYS}=10MHz</th><th>Unit</th></tr>
<tr><td>00</td><td>6</td><td>3</td><td rowspan="4">μs</td></tr>
<tr><td>01</td><td>13</td><td>6</td></tr>
<tr><td>10</td><td>26</td><td>13</td></tr>
<tr><td>11</td><td>51</td><td>26</td></tr>
</table>
</td></tr>
</table>

22.4 LED display RAM

Both General LED and Bidirectional drive mode LED use Automatic Scanning, and their RAM addresses are multiplexed:

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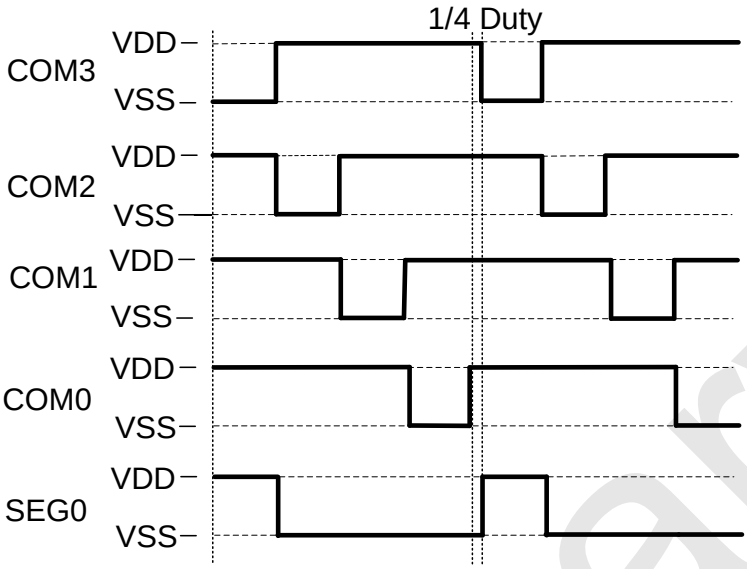


22.4.1 General LED display RAM (400H to 40FH) @ DMOD=0

Address	Register Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
400H	COM0	S7	S6	S5	S4	S3	S2	S1	S0
401H		-	-	-	-	S11	S10	S9	S8
402H	COM1	S7	S6	S5	S4	S3	S2	S1	S0
403H		-	-	-	-	S11	S10	S9	S8
404H	COM2	S7	S6	S5	S4	S3	S2	S1	S0
405H		-	-	-	-	S11	S10	S9	S8
406H	COM3	S7	S6	S5	S4	S3	S2	S1	S0
407H		-	-	-	-	S11	S10	S9	S8
408H	COM4	S7	S6	S5	S4	S3	S2	S1	S0
409H		-	-	-	-	S11	S10	S9	S8
40AH	COM5	S7	S6	S5	S4	S3	S2	S1	S0
40BH		-	-	-	-	S11	S10	S9	S8
40CH	COM6	S7	S6	S5	S4	S3	S2	S1	S0
40DH		-	-	-	-	S11	S10	S9	S8
40EH	COM7	S7	S6	S5	S4	S3	S2	S1	S0
40FH		-	-	-	-	S11	S10	S9	S8

22.4.1.1 LED Waveform

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Waveform Diagram of COM and SEG in LED Applications

22.4.2 Bidirectional drive mode LED display RAM (400H to 417H) @ DMOD=1

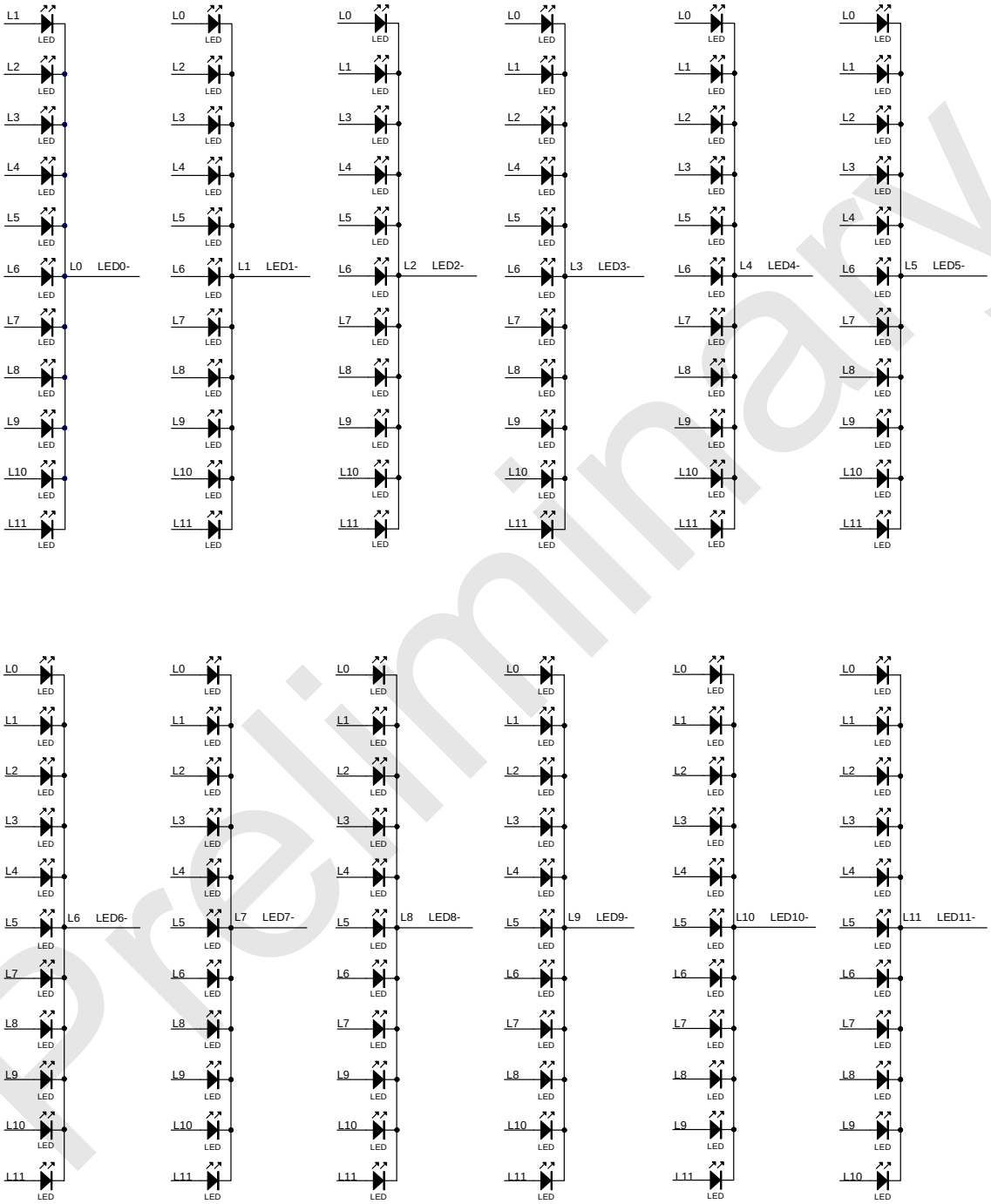
Note: Each byte from 408H to 40FH has all 8 bits valid

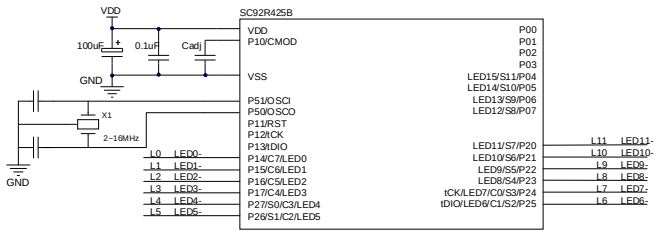
Address	Register Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
400H	LED0-	7	6	5	4	3	2	1	-
401H		-	-	-	-	11	10	9	8
402H	LED1-	19	18	17	16	15	14	-	0
403H		-	-	-	-	23	22	21	20
404H	LED2-	31	30	29	28	27	-	13	12
405H		-	-	-	-	35	34	33	32
406H	LED3-	43	42	41	40	-	26	25	24
407H		-	-	-	-	47	46	45	44
408H	LED4-	55	54	53	-	39	38	37	36
409H		-	-	-	-	59	58	57	56
40AH	LED5-	67	66	-	52	51	50	49	48
40BH		-	-	-	-	71	70	69	68
40CH	LED6-	79	-	65	64	63	62	61	60
40DH		-	-	-	-	83	82	81	80
40EH	LED7-	-	78	77	76	75	74	73	72
40FH		-	-	-	-	95	94	93	92
410H	LED8-	91	90	89	88	87	86	85	84
411H		-	-	-	-	107	106	105	-
412H	LED9-	103	102	101	100	99	98	97	96
413H		-	-	-	-	119	118	-	104
414H	LED10-	115	114	113	112	111	110	109	108
415H		-	-	-	-	131	-	117	116
416H	LED11-	127	126	125	124	123	122	121	120
417H		-	-	-	-	-	130	129	128

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22.4.3 Bidirectional drive mode LED hardware connection example

Ln in the figure below is the Segment Output corresponding to LEDn, and the Valid Output is constant current; LEDn- is the Bit scanning corresponding to LEDn, with an active level of Low level.





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During the Valid Output Scan Interval of LEDn-, the LEDn driver outputs a Low level signal (n=0, 1, 2.....11), while the output signals of the other LED drivers are determined by the Display data:

- When the Display data is "1", the corresponding LED driver outputs a high-level signal
- When the Display data is "0", the corresponding LED driver enters a high-impedance state (also known as a floating state)
- When scanning LEDn-, the corresponding LEDn- outputs a Low level.

To prevent LED flicker when switching the LEDn- Scan Interval, the LED driver is equipped with adjustable Dead Time. During dead time, the LED driver briefly outputs an inactive signal.

To ensure display quality, the LED Dead Time should be set within 10 µs to 3 µs as much as possible. The following three cases are recommended:

1. LEDCK=00, System Clock Frequency 5 MHz, Dead Time 6 µs
2. LEDCK=00, System Clock Frequency 10 MHz, Dead Time 3 µs
3. LEDCK=01, System Clock Frequency 10 MHz, Dead Time 6 µs.

The LED Dead Time is related to LEDCK[1:0] and System Clock Frequency f_{SYS}, as shown in the table below:

LEDCK[1:0]	f_{SYS}=5 MHz	f_{SYS}=10 MHz	Unit
00	6	3	µs
01	13	6	
10	26	13	
11	51	26	

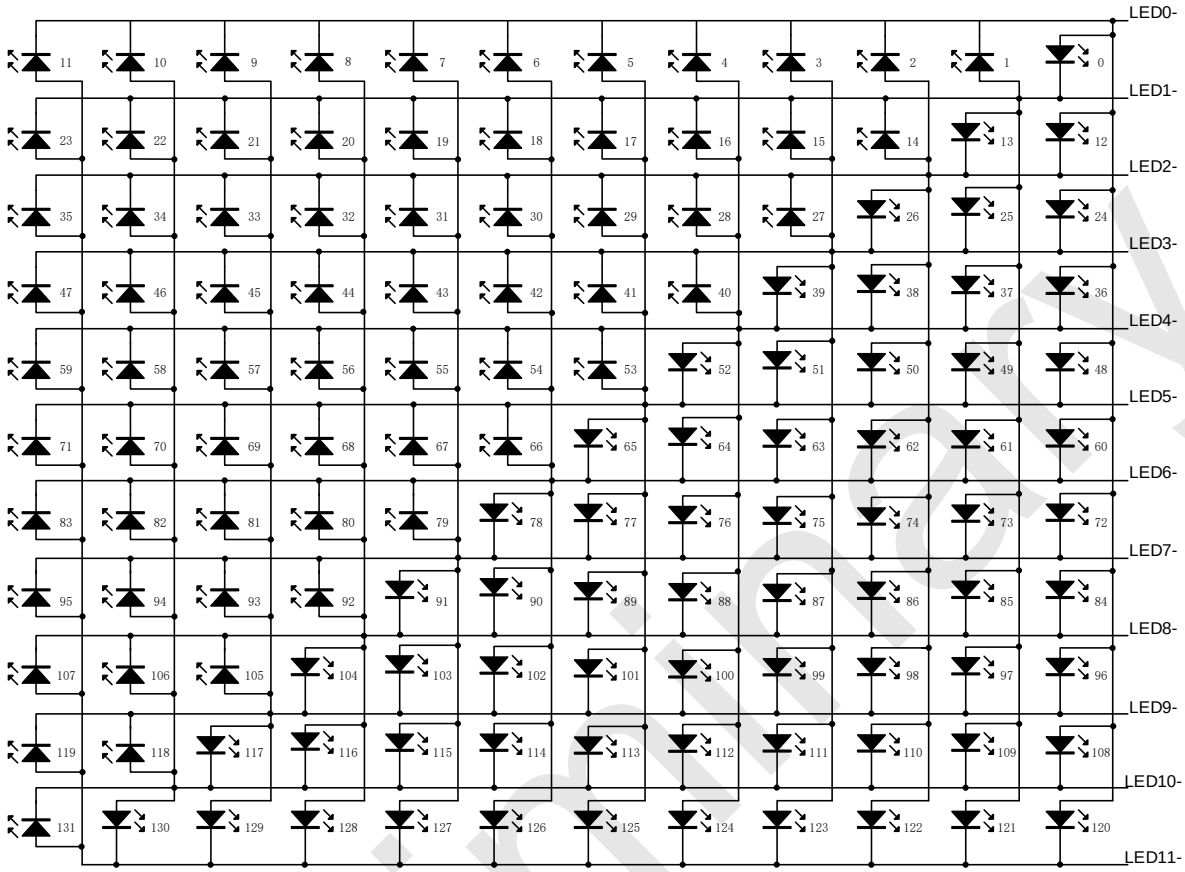
The correspondence between Display data, Address, and Chip Pins (LEDn) is shown in the table below (Ln is the Segment Output corresponding to LEDn, and the Valid Output is constant current; LEDn - bit scan corresponding to LEDn; active Low level):

bit	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	LEDn Port scanning
Address	L11	L10	L9	L8	L7	L6	L5	L4	L3	L2	L1	L0	
400H	11	10	9	8	7	6	5	4	3	2	1	_	LED0-
402H	23	22	21	20	19	18	17	16	15	14	_	0	LED1-
404H	35	34	33	32	31	30	29	28	27	_	13	12	LED2-
406H	47	46	45	44	43	42	41	40	_	26	25	24	LED3-
408H	59	58	57	56	55	54	53	_	39	38	37	36	LED4-
40AH	71	70	69	68	67	66	_	52	51	50	49	48	LED5-
40CH	83	82	81	80	79	_	65	64	63	62	61	60	LED6-
40EH	95	94	93	92	_	78	77	76	75	74	73	72	LED7-
410H	107	106	105	_	91	90	89	88	87	86	85	84	LED8-
412H	119	118	_	104	103	102	101	100	99	98	97	96	LED9-
414H	131	_	117	116	115	114	113	112	111	110	109	108	LED10-
416H	_	130	129	128	127	126	125	124	123	122	121	120	LED11-

In the table above, the numbers in the white cells correspond one-to-one with the LED numbers in the figure below:

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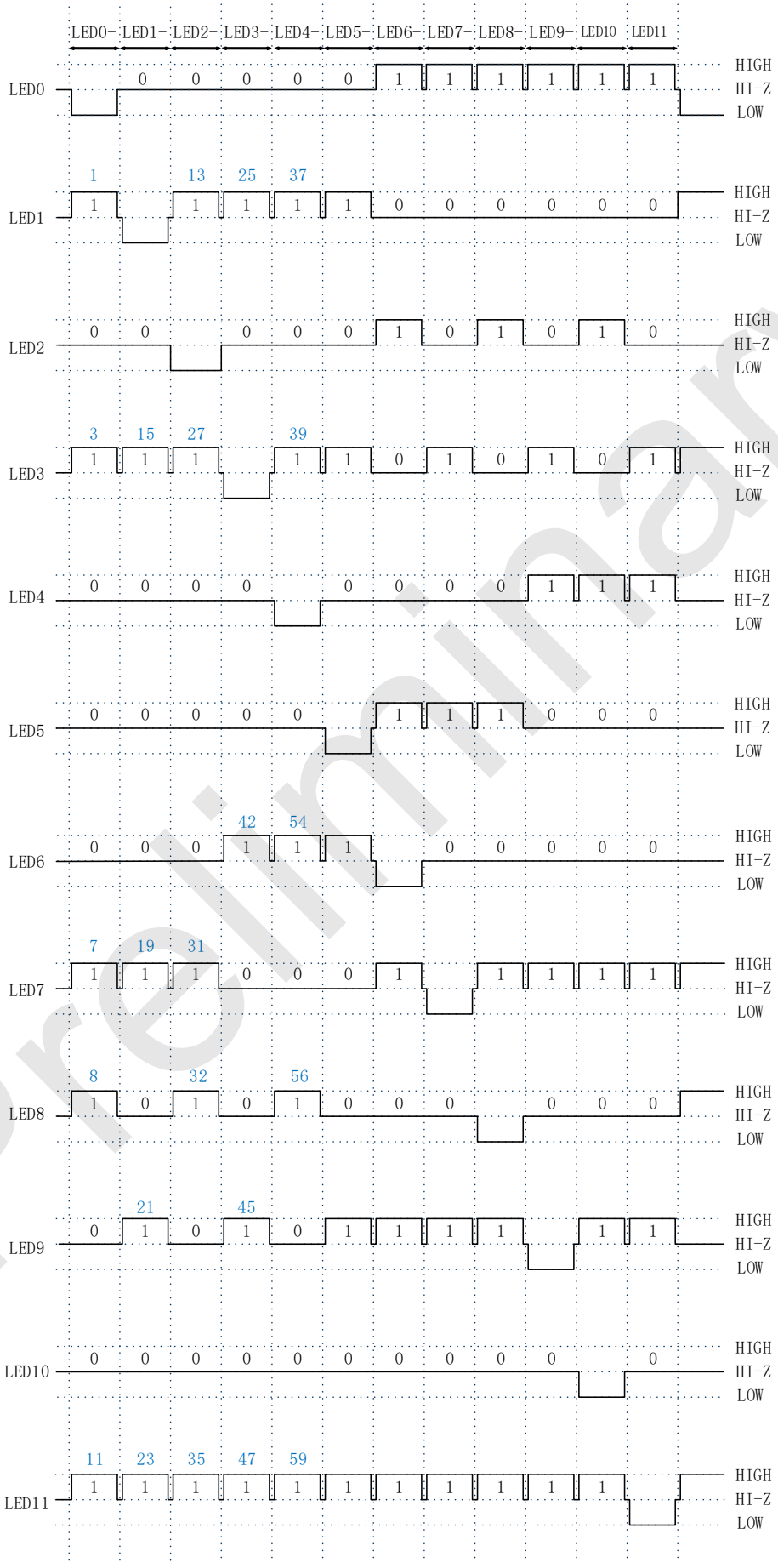
22.4.4 Bidirectional drive scan timing



22.4.5 Scan timing example

The blue numbers in the figure below correspond to the LED numbers in the Bidirectional drive scan timing diagram. The LEDs lit while scanning from LED0- to LED4- are as follows:

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23 Electrical characteristics

23.1 Absolute maximum ratings

Symbol	Parameter	Minimum	Maximum	UNIT
V_{DD}/V_{SS}	DC supply voltage	-0.3	6	V
Voltage ON any Pin	Input/output voltage at any Pin	-0.3	V_{DD}+0.3	V
T_A	Operating ambient temperature	-40	105	℃
T_{STG}	Storage temperature	-55	125	℃
I_{VDD}	Current flowing through V_{DD}	-	200	mA
I_{VSS}	Current flowing through V_{SS}	-	200	mA

23.2 Recommended operating conditions

Symbol	Parameter	Minimum	Maximum	UNIT
V_{DD}	Operating Voltage	2.4	5.5	V
T_A	Operating ambient temperature	-40	105	℃

23.3 Flash ROM parameters

Symbol	Parameter	Minimum	Typical Value	Maximum	UNIT	Condition
N_{END}	Erase/Write Cycles	10,000	-	-	Cycles	
T_{DR}	Data Retention Time	10	-	-	Years	T_A = +25℃
$T_{S-Erase}$	Single Sector Erase Time	-	7	-	ms	T_A = +25℃ Fast Erase Area
		-	30	-	ms	T_A = +25℃ Non-Fast Erase Area
$T_{P-Erase}$	Single-Page Erase Time	-	30	-	ms	T_A = +25℃
T_{Erase}	Chip Erase Time	-	30	-	ms	T_A = +25℃
T_{Write}	Single-Byte Write Time	-	100	-	μs	T_A = +25℃

23.4 DC electrical characteristics

(VDD = 5 V,TA = +25 ℃,Description)

Symbol	Parameter	Minimum	Typical Value	Maximum	Unit	Condition
Current						
I_{op1}	Operating current	-	2.6	-	mA	f_{SYS} =10 MHz
I_{op2}	Operating current	-	2.0	-	mA	f_{SYS} =5 MHz
I_{op3}	Operating current	-	1.6	-	mA	f_{SYS} =1.66 MHz
I_{pd1}	Standby Current (Power-Down mode)	-	2.3	-	μA	
I_{IDL1}	Standby Current (IDLE mode)	-	1.9	-	mA	
I_{BTM}	Base Timer operating current	-	1	2	μA	BTMFS[3:0]=1000 Generates an

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Symbol	Parameter	Minimum	Typical Value	Maximum	Unit	Condition
						interrupt every 4.0 seconds
I_{WDT}	WDT current	-	1	2	μA	WDTCKS[2:0]=000 WDT overflow time: 500 ms
I_{TK1}	High-sensitivity Touch key operating current	-	0.6	1	mA	
I_{WL1}	Water Level operating current	-	0.6	1	mA	
I/O characteristics						
V_{IH1}	Input high voltage	0.7 V_{DD}	-	V_{DD}+0.3	V	
V_{IL1}	Input low voltage	-0.3	-	0.3 V_{DD}	V	
V_{IH2}	Input high voltage	0.8 V_{DD}	-	V_{DD}	V	Schmitt-Trigger Input: NRST tCK / tDIO UART0 input RXD0 SSI signal input INT0 to 1 Timer clock input, Timer Capture Port
V_{IL2}	Input low voltage	-0.2	-	0.2 V_{DD}	V	
I_{OL1}	Low output current P00 to P03 P10 to P13 P50, P51	-	42	-	mA	V_{Pin} =0.4 V
I_{OL2}	Low output current P00 to P03 P10 to P13 P50, P51	-	76	-	mA	V_{Pin} =0.8 V
I_{OL3}	Low output current P04 to P07 P14 to P17 P20 to P27	-	80	-	mA	V_{Pin} =0.4 V
I_{OL4}	Low output current P04 to P07 P14 to P17 P20 to P27	-	145	-	mA	V_{Pin} =0.8 V
I_{LED_OL1}	LED Pin Sink Current Drive (single) (0.4 V)	-	80	-	mA	V_{LED} = 0.4V
I_{LED_OL2}	LED Pin Sink Current Drive (single) (0.8 V)	-	150	-	mA	V_{LED} = 0.8V
I_{OH1}	High output current P00 to P03 P10 to P13 P50, P51	-	16	-	mA	V_{Pin}=4.3 V
I_{OH2}	High output current P00 to P03 P10 to P13 P50, P51	-	7	-	mA	V_{Pin}=4.7 V
I_{OH3}	High output current P04 to P07 P14 to P17 P20 to P27	-	19	-	mA	V_{Pin}=4.3 V
I_{OH4}	High output current P04 to P07 P14 to P17 P20 to P27	-	9	-	mA	V_{Pin}=4.7 V

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Symbol	Parameter	Minimum	Typical Value	Maximum	Unit	Condition
I_{lkg1}	Input leakage current	-1	-	1	μA	IO in High-impedance input mode V_{IN}= V_{DD} or V_{SS}
R_{PH1}	Pull-up resistor	16.5	33	49.5	kΩ	V_{IN} = V_{SS}

(VDD = 3.3 V, TA = +25 ℃, unless otherwise specified)

Symbol	Parameter	Minimum	Typical Value	Maximum	Unit	Condition
Current						
I_{op4}	Operating current	-	2.4	-	mA	f_{SYS} =10 MHz
I_{op5}	Operating current	-	1.9	-	mA	f_{SYS} =5 MHz
I_{op6}	Operating current	-	1.5	-	mA	f_{SYS} =1.66 MHz
I_{pd2}	Standby Current (Power-Down mode)	-	2.1	-	μA	
I_{IDL2}	Standby Current (IDLE mode)	-	1.9	-	mA	
I_{TK2}	High-sensitivity Touch key operating current	-	0.6	1	mA	
I_{WL2}	Water Level operating current	-	0.6	1	mA	
I/O characteristics						
V_{IH3}	Input high voltage	0.7 V_{DD}	-	V_{DD}+0.3	V	
V_{IL3}	Input low voltage	-0.3	-	0.3 V_{DD}	V	
V_{IH4}	Input high voltage	0.8 V_{DD}	-	V_{DD}	V	Schmitt-Trigger Input: NRST tCK / tDIO UART0 input RXD0 SSI signal input INT0 to 1 Timer clock input Timer Capture Port
V_{IL4}	Input low voltage	-0.2	-	0.2 V_{DD}	V	
I_{OL5}	Low output current P00 to P03 P10 to P13 P50, P51	-	30	-	mA	V_{Pin} =0.4 V
I_{OL6}	Low output current P00 to P03 P10 to P13 P50, P51	-	50	-	mA	V_{Pin}=0.8 V
I_{OL7}	Low output current P04 to P07 P14 to P17 P20 to P27	-	60	-	mA	V_{Pin} =0.4 V
I_{OL8}	Low output current P04 to P07 P14 to P17 P20 to P27	-	105	-	mA	V_{Pin}=0.8 V
I_{LED_OL3}	LED Pin Sink Current Drive (single) (0.4 V)	-	60	-	mA	V_{LED}=0.4 V
I_{LED_OL4}	LED Pin Sink Current Drive (single) (0.8 V)	-	105	-	mA	V_{LED}=0.8 V
I_{OH5}	High output current P00 to P03 P10 to P13 P50, P51	-	5	-	mA	V_{Pin}=3.0 V

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Symbol	Parameter	Minimum	Typical Value	Maximum	Unit	Condition
I_{OH6}	High output current P04 to P07 P14 to P17 P20 to P27	-	6	-	mA	V_{Pin}=3.0 V
I_{lkg2}	Input leakage current	-1	-	1	μA	IO in High-impedance input mode V_{IN}= V_{DD} or V_{SS}
R_{PH2}	Pull-up resistor	28	56	84	kΩ	V_{IN} = V_{SS}

23.5 LED electrical characteristics

(VDD = 5 V,TA = +25 ℃,Description)

Symbol			Parameter	Minimum	Typical Value	Maximum	Unit	Condition
D_{LED_OUT}			Output Current Error	-	-	±5%	mA	V_{LED} = 2 V
ΔI1			Line Regulation	-	-	±3	%/V	
ΔI2			Load Regulation	-	-	±3	%/V	
ΔT			Temperature Drift	-	-	±3	%/V	
Symbol	**No.**	**DRIV[3:0]**	**Parameter**	**Minimum**	**Typical Value**	**Maximum**	**Unit**	**Condition**
I_{LED_OH1}	0	0000	Brightness Level 1	-	1.25	-	mA	V_{LED} = 2 V
	1	0001	Brightness Level 2	-	2.50	-	mA	
	2	0010	Brightness Level 3	-	3.75	-	mA	
	3	0011	Brightness Level 4	-	5.00	-	mA	
	4	0100	Brightness Level 5	-	6.25	-	mA	
	5	0101	Brightness Level 6	-	7.50	-	mA	
	6	0110	Brightness Level 7	-	8.75	-	mA	
	7	0111	Brightness Level 8	-	10.00	-	mA	
	8	1000	Brightness Level 9	-	11.25	-	mA	
	9	1001	Brightness Level 10	-	12.50	-	mA	
	10	1010	Brightness Level 11	-	13.75	-	mA	
	11	1011	Brightness Level 12	-	15.00	-	mA	
	12	1100	Brightness Level 13	-	16.25	-	mA	
	13	1101	Brightness Level 14	-	17.50	-	mA	
	14	1110	Brightness Level 15	-	18.75	-	mA	

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Symbol			Parameter	Minimum	Typical Value	Maximum	Unit	Condition
	15	1111	Brightness Level 16	-	20.00	-	mA	
	16	CMED=0	/	-	21.25	-	mA	

23.6 AC electrical characteristics

(VDD = 2.4 V to 5.5 V, TA = 25 ℃, unless otherwise specified)

Symbol	Parameter	Minimum	Typical Value	Maximum	Unit	Condition
T_{osc1}	External high-frequency oscillator startup time	-	9	-	ms	External 16 MHz crystal
T_{osc2}	External high-frequency oscillator startup time	-	18	-	ms	External 8 MHz crystal
T_{osc3}	External high-frequency oscillator startup time	-	35	-	ms	External 4 MHz crystal
T_{POR}	Power-On Reset time	-	15	-	ms	
T_{PDW}	Power-Down mode wake-up time	-	60	130	μs	
T_{Reset}	Reset pulse width	18	-	-	μs	active low
T_{LVR}	LVR Debounce Time	-	30	-	μs	
f_{HRC}	RC Oscillator Stability	19.8	20	20.2	MHz	V_{DD}=2.4 to 5.5 V T_A=-20 to 85 ℃

23.7 ADC electrical characteristics

(TA = 25°C, unless otherwise specified)

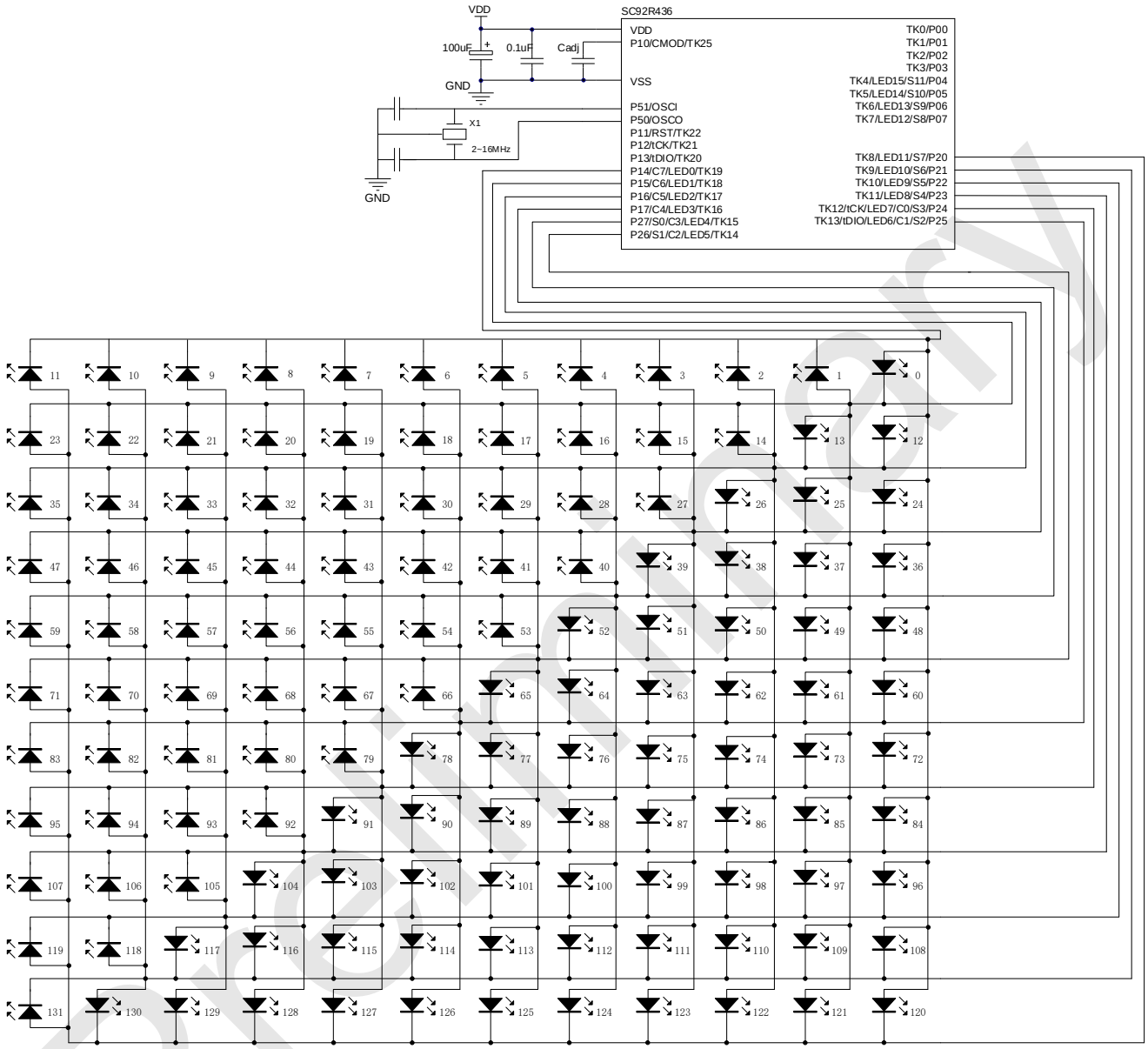
Symbol	Parameter	Minimum	Typical Value	Maximum	Unit	Condition
V_{AD1}	Supply voltage 1	2.4	5.0	5.5	V	V_{ref}=V_{DD} or 1.024 V
V_{AD2}	Supply voltage 2	2.4	5.0	5.5	V	V_{ref}=2.048 V
V_{AD3}	Supply voltage 3	2.7	5.0	5.5	V	V_{ref}=2.4 V
V_{REF1}	1.024 V Internal Reference	1.004	1.024	1.044	V	V_{DD} = 2.4 to 5.5 V
V_{REF2}	2.4 V Internal Reference	2.38	2.40	2.42	V	V_{DD} = 2.7 to 5.5 V
V_{REF3}	2.048 V Internal Reference	2.028	2.048	2.068	V	V_{DD} = 2.4 to 5.5 V
N_R	Accuracy	-	12	-	bit	GND≤V_{AIN}≤V_{DD}
V_{AIN}	ADC input voltage	GND	-	V_{DD}	V	
R_{AIN}	ADC input resistance	1	-	-	MΩ	V_{IN}=5 V
I_{lkg_ADC}	ADC input leakage current	-1	-	1	μA	V_{IN}= V_{AINx}
I_{ADC1}	ADC Conversion Current 1	-	1.4	1.8	mA	ADC module enabled V_{DD}=5 V
I_{ADC2}	ADC Conversion Current2	-	1.1	1.5	mA	ADC module enabled V_{DD}=3.3 V
DNL	Differential Nonlinearity Error	-	±1	-	LSB	V_{DD}=5 V V_{REF}=5 V
INL	Integral Nonlinearity Error	-	±2	-	LSB	
E_Z	Offset Error	-	±2	-	LSB	
E_F	Full-Scale Error	-	±3	-	LSB	
E_{AD}	Total Absolute Error	-	±3	-	LSB	

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Symbol	Parameter	Minimum	Typical Value	Maximum	Unit	Condition
T_{ADC1}	ADC sampling + Total Conversion Time1	-	8.4	27.6	μs	f_{SYS}=10 MHz LOWSP[2:0] = 000
T_{ADC2}	ADC sampling + Total Conversion Time2	-	11.4	30.6	μs	f_{SYS}=10 MHz LOWSP[2:0] = 001
T_{ADC3}	ADC sampling + Total Conversion Time3	-	8.4	27.6	μs	f_{SYS}=10 MHz LOWSP[2:0] = 010
T_{ADC4}	ADC sampling + Total Conversion Time4	-	11.4	30.6	μs	f_{SYS}=10 MHz LOWSP[2:0] = 011

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24 Application circuit



SC92R425B bidirectional drive mode LED application circuit

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25 Ordering information

PRODUCT NUMBER	PACKAGE	PACKING
SC92R425BX28U	TSSOP28	Tube
SC92R425BM28U	SOP28	Tube
SC92R425BX20U	TSSOP20	Tube
SC92R425BM20U	SOP20	Tube
SC92R425BM16U	SOP16	Tube
SC92R425BM08U	SOP8	Tube
SC92R425BX28T	TSSOP28	Tape and Reel
SC92R425BM28T	SOP28	Tape and Reel
SC92R425BX20T	TSSOP20	Tape and Reel
SC92R425BM20T	SOP20	Tape and Reel
SC92R425BM16T	SOP16	Tape and Reel
SC92R425BM08T	SOP8	Tape and Reel

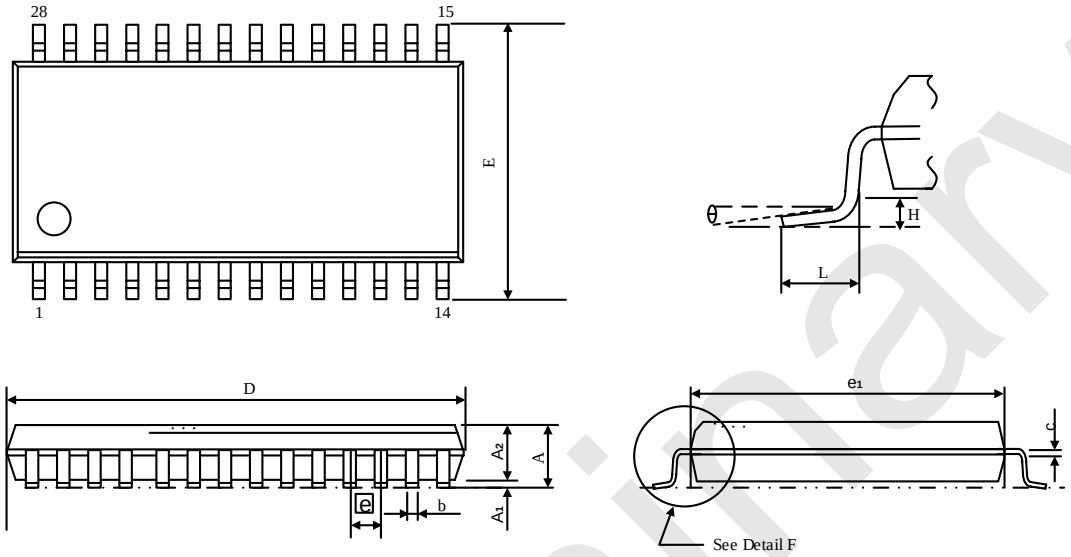
Note: For mass-production availability of specific models, please consult SinOne or its distributors about sample availability and delivery timelines before starting development.

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26 Package information

SC92R425BX28U, SC92R425BX28T

TSSOP28L Dimensions (unit: mm)

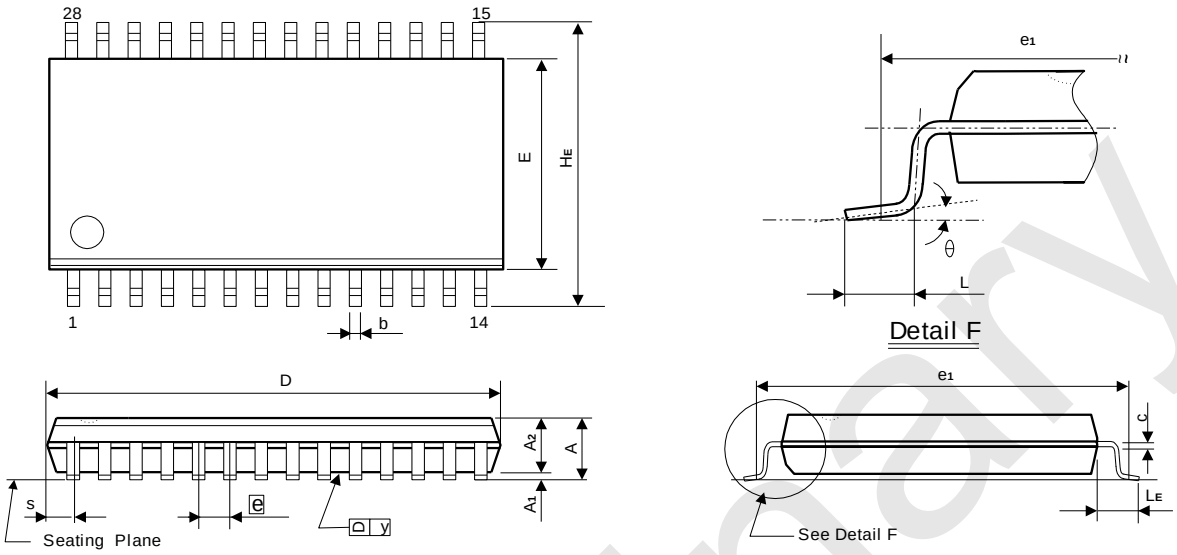


Symbol	mm (millimeters)		
	Min	Typ	Max
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	0.900	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	9.600	9.700	9.800
E	6.250	6.400	6.550
e1	4.300	4.400	4.500
e	0.65 (BSC)		
L	-	-	1.0
θ	0°	-	8°
H	0.05	-	0.25

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SC92R425BM28U,SC92R425BM28T

SOP28L (300mil) Dimensions (unit: mm)

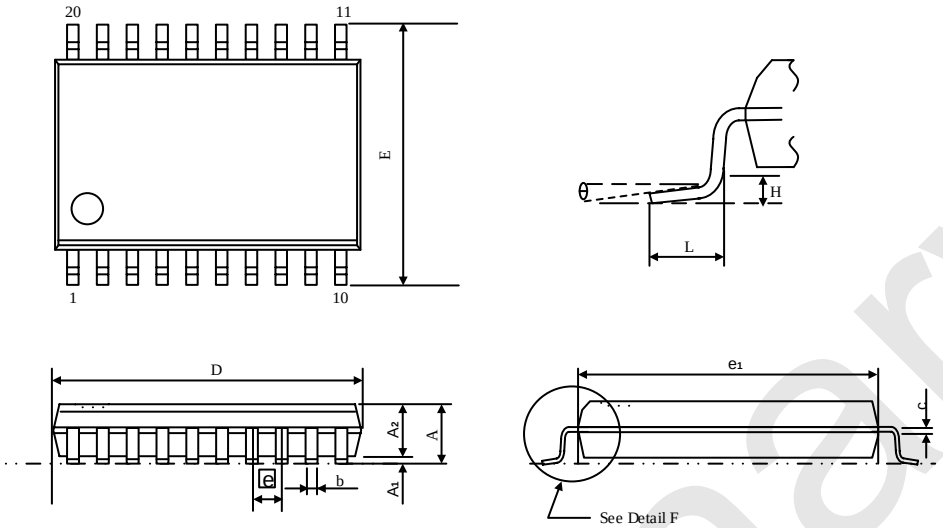


Symbol	mm (millimeters)		
	Min	Typ	Max
A	2.40	2.56	2.65
A1	0.100	0.200	0.300
A2	2.240	2.340	2.440
b	0.39	---	0.48
C	0.254 (BSC)		
D	17.80	18.00	18.20
E	7.30	7.50	7.70
HE	10.100	10.300	10.500
e	1.270 (BSC)		
L	0.7	0.85	1.0
LE	1.3	1.4	1.5
θ	0°	-	8°

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SC92R425BX20U,SC92R425BX20T

TSSOP20L Dimensions (unit: mm)

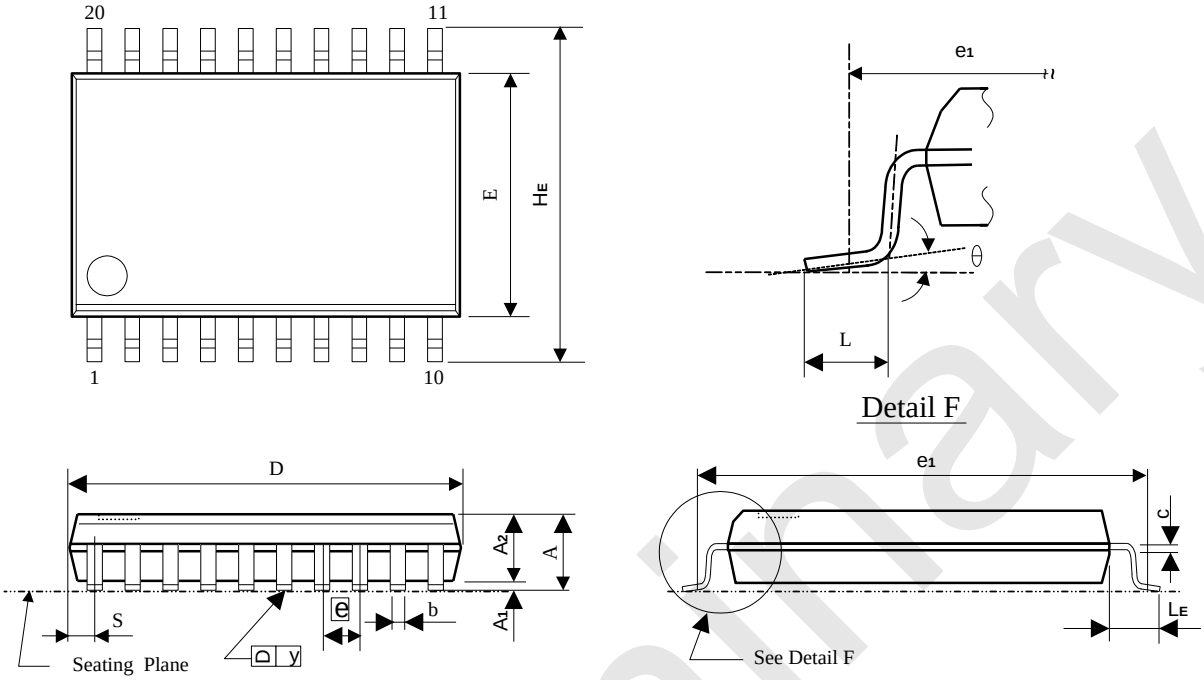


Symbol	mm (millimeters)		
	Min	Typ	Max
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	6.400	-	6.600
E	6.20	-	6.60
e1	4.300	-	4.500
e	0.65 (BSC)		
L	-	-	1.00
θ	0°	-	8°
H	0.05	-	0.15

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SC92R425BM20U,SC92R425BM20T

SOP20L (300mil) Dimensions (unit: mm)

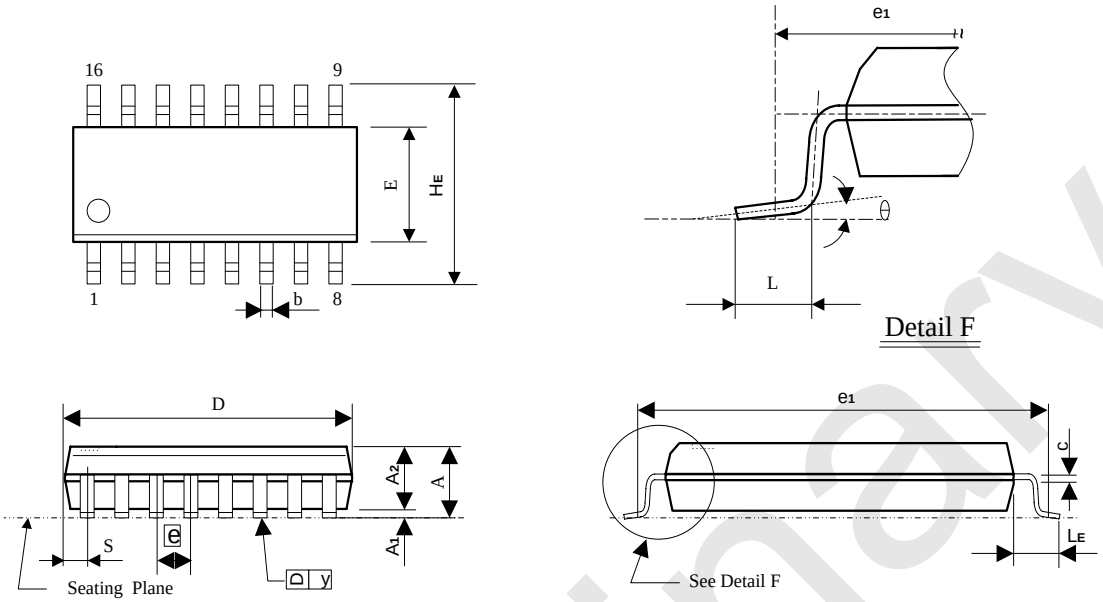


Symbol	mm (millimeters)		
	Min	Typ	Max
A	2.40	2.56	2.65
A1	0.100	0.200	0.300
A2	2.240	2.340	2.440
b	0.35	--	0.47
c	0.25	--	0.31
D	12.60	12.80	13.00
E	7.30	7.50	7.70
HE	10.100	10.300	10.500
e	1.27 (BSC)		
L	0.700	0.850	1.000
LE	1.30	1.40	1.50
θ	0°	-	8°

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SC92R425BM16U,SC92R425BM16T

SOP16L (150mil) Dimensions (unit: mm)

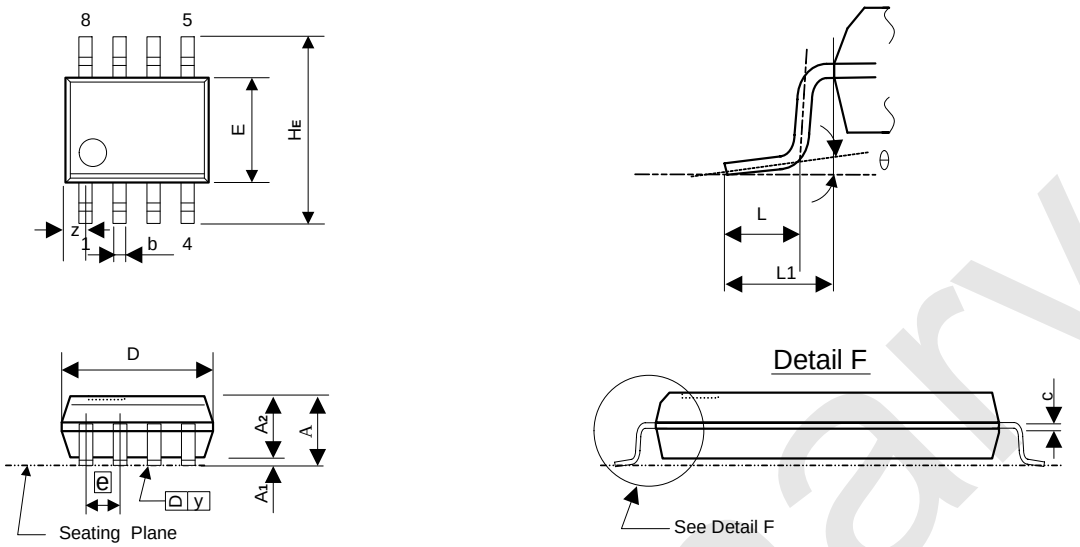


Symbol	mm (millimeters)		
	Min	Typ	Max
A	1.500	1.625	1.750
A1	0.050	0.1375	0.225
A2	1.30	1.45	1.55
b	0.38	0.43	0.48
c	0.20	0.23	0.26
D	9.70	9.90	10.10
E	3.70	3.90	4.10
HE	5.80	6.00	6.20
e		1.27 (BSC)	
L	0.50	0.65	0.80
LE	0.95	1.05	1.15
θ	0°	-	8°

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SC92R425BM08U,SC92R425BM08T

SOP8L (150mil) Dimensions (unit: mm)



Symbol	mm (millimeters)		
	Min	Typ	Max
A	1.500	1.625	1.750
A1	0.100	0.1625	0.225
A2	1.30	1.425	1.55
b	0.39	0.435	0.48
c	0.20	0.23	0.26
D	4.70	4.90	5.10
E	3.70	3.90	4.10
HE	5.80	6.00	6.20
e	1.270 (BSC)		
L	0.50	0.65	0.80
LE	0.95	1.05	1.15
θ	0°	-	8°

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27 Revision history

Version	Record	Date
V0.1	Initial Release	August 5, 2026

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Important notice

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